PRINCETON UNIVERSITY

Inductor-Linked Multi-Output Switched-Capacitor Power Architecture for High Current Chiplets

Mian Liao[+], Daniel Zhou[+], Ping Wang, Minjie Chen

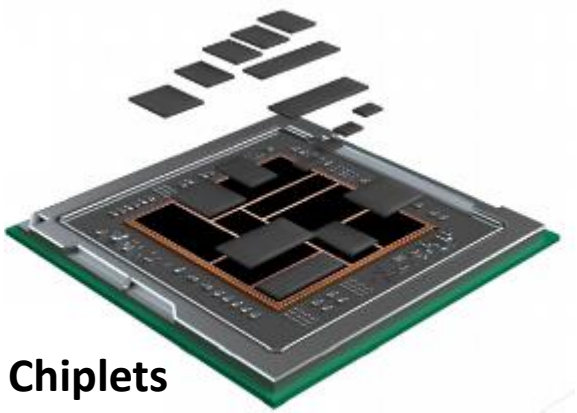
Department of Electrical and Computer Engineering

Andlinger Center for Energy and the Environment

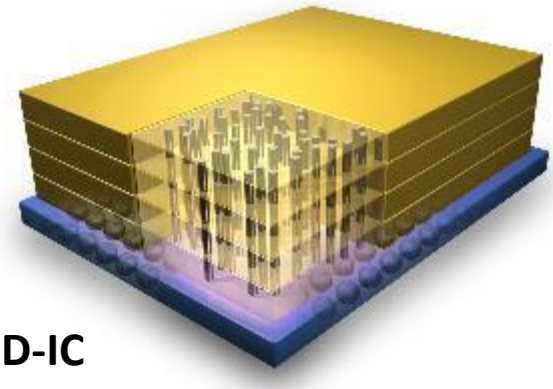
Princeton University

[+]M. Liao and D. Zhou contributed equally to the paper and the presentation

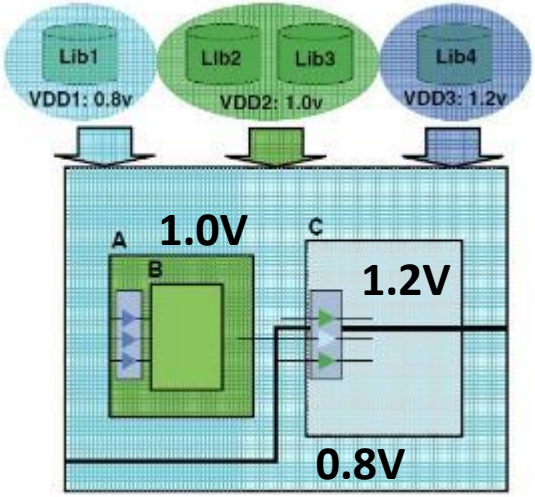
Power Delivery Challenges of High Current Chiplets



Chiplets



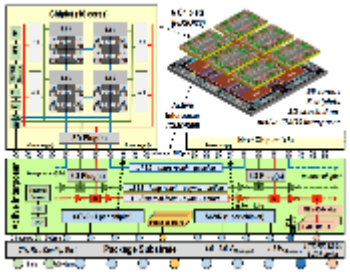
3D-IC

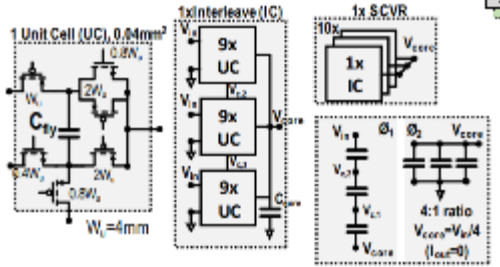


- High power, higher input voltage (48 V), lower output voltage (<0.5 V)
- Multiple individually regulated output voltages: 0.8V, 1.8V, 3.3V, etc.
- Significant variation in bus voltage (>40%) due to complicated PDN
- Sophisticated voltage regulation requirements: dynamics, ripple, noise
- Efficiency, power density, packaging, signal/power integrity

Power Delivery Solutions for Chiplet Systems

Low Power Low Conversion Ratio Capacitor-based





IntAct: Off-chip VRM + in-substrate SwCap

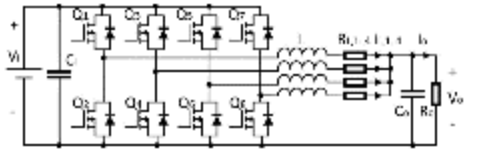
- Input: 0.9V to 2.9V
- Output: 0.4V to 1.8V
- Power: 2.6W

P. Vivet *et al*., "IntAct: A 96-Core Processor With Six Chiplets 3D-Stacked on an Active Interposer With Distributed Interconnects and Integrated Power Management," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 1, pp. 79-97, Jan. 2021.

High Power High Conversion Ratio Inductor-based

Tesla Dojo

MPC22161



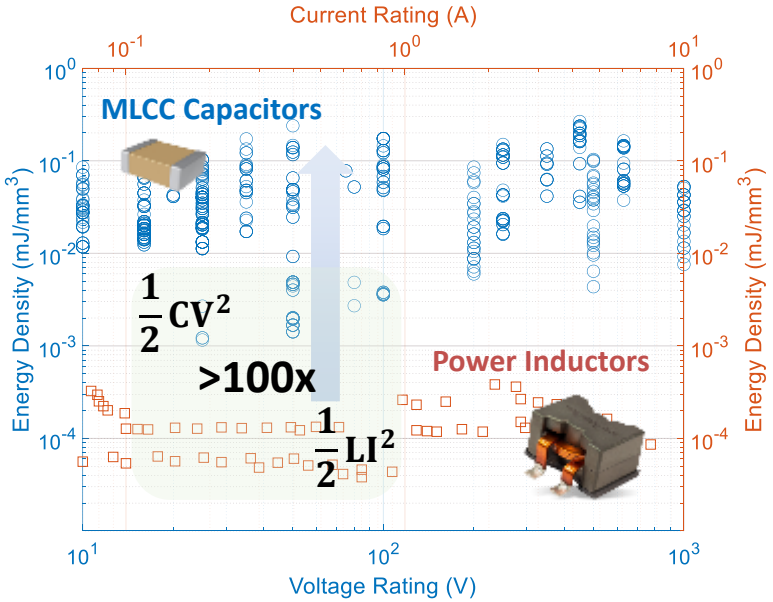
MPS Vertical Power Module

- Input: 4V to 16V
- Output: 0.5V to 1V
- Current: 120A

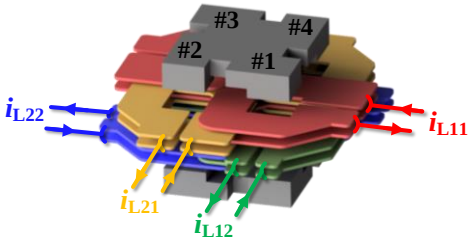
High Conversion Ratio Hybrid SwCap Multi-Output Designs

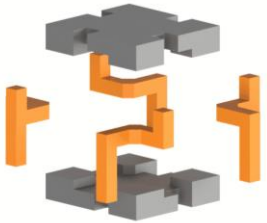
PRINCETON UNIVERSITY

Capacitors : high density, high Q



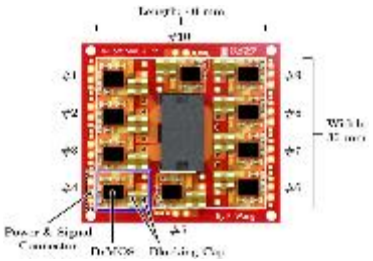
Magnetics : design flexibility & functionality





Ripple Cancellation

CM/DM Choke



Turns Ratio

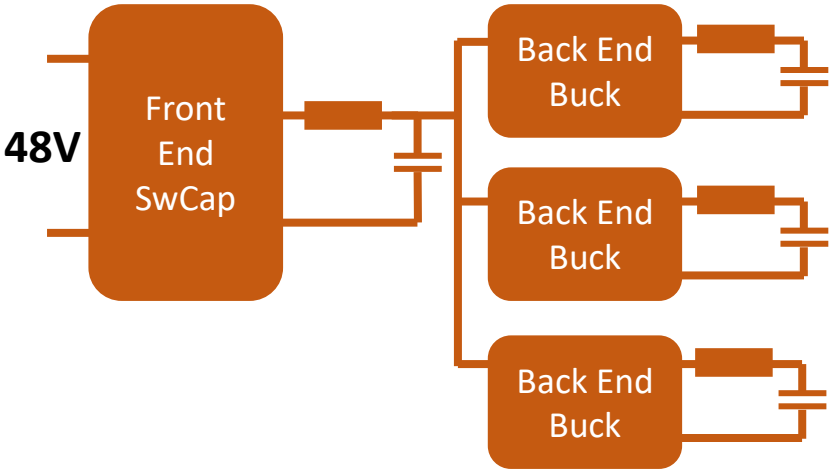
Galvanic Isolation

EMI Filter

- *Sullivan et al., "On Size and Magnetics: Why Small Efficient Power Inductors are Rare," 3D-PEIM'16.*
- *Sullivan and Chen, "Coupled Inductors for Fast-Response High-Density Power Delivery: Discrete and Integrated," CICC'21.*
- *Kyaw et al., "Fundamental Examination of Multiple Potential Passive Component Technologies …," TPEL'18.*

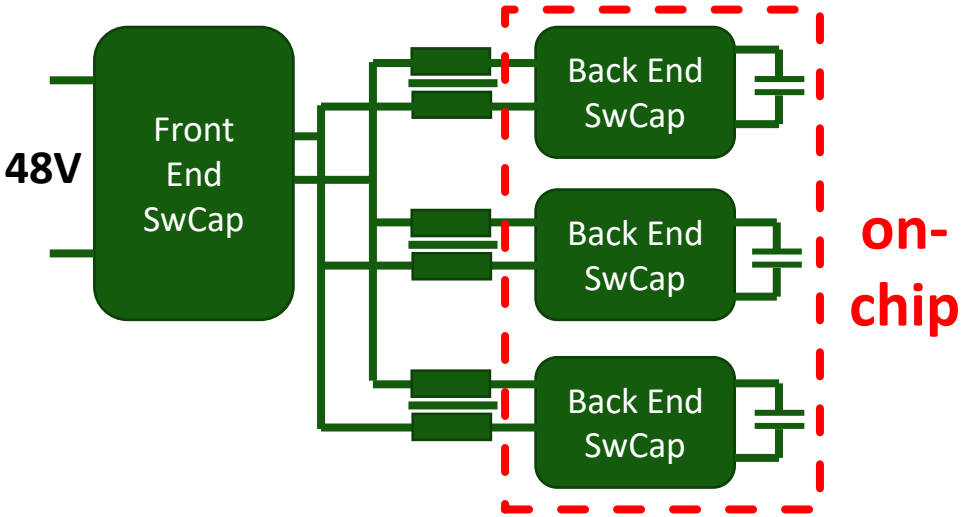
DC Intermediate Bus versus AC Intermediate Bus

Two-Stage Design with Capacitor-Link



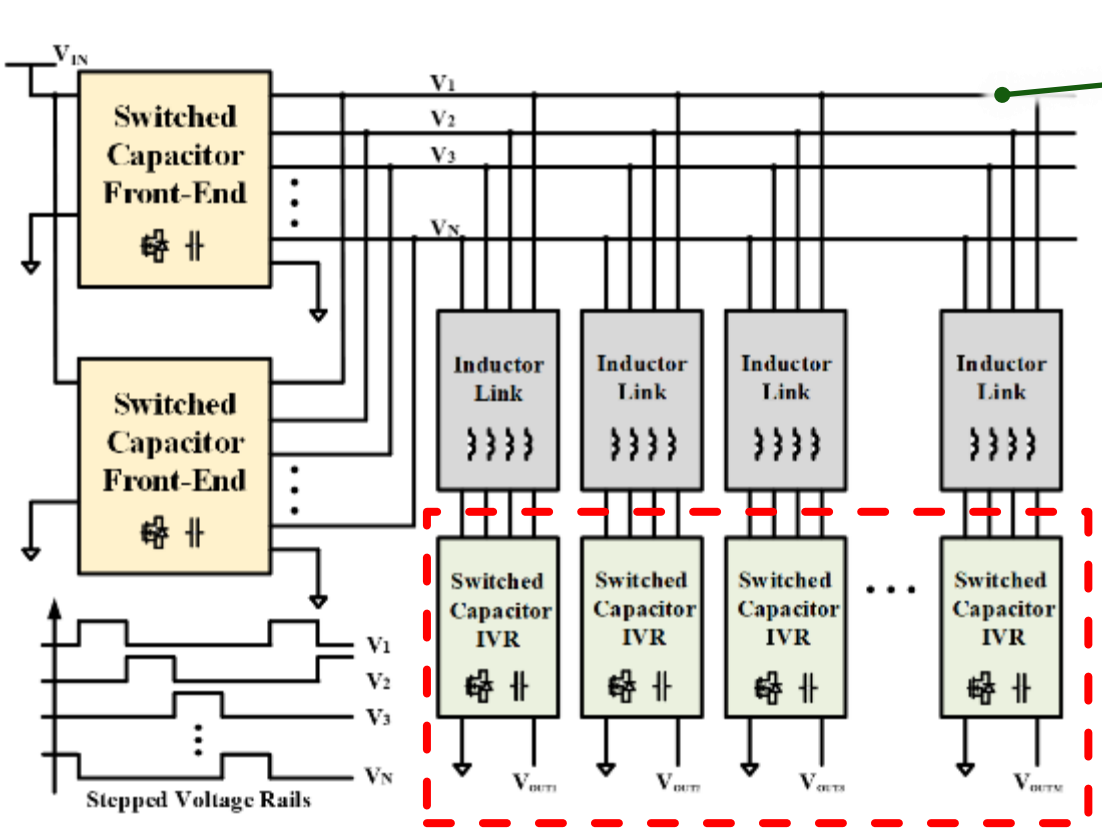
1) Need on-chip inductors
2) Large bus capacitor & inductor
3) Tightly regulated intermediate bus

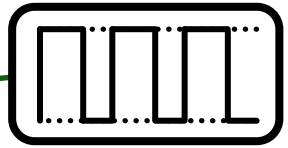
Two-Stage Design with Inductor-Link



1) Integrated back-end w/ on-chip capacitors
2) No bus capacitor, coupled inductor links
3) Unregulated intermediate bus

Modular Building Blocks for the Inductor-Link Architecture

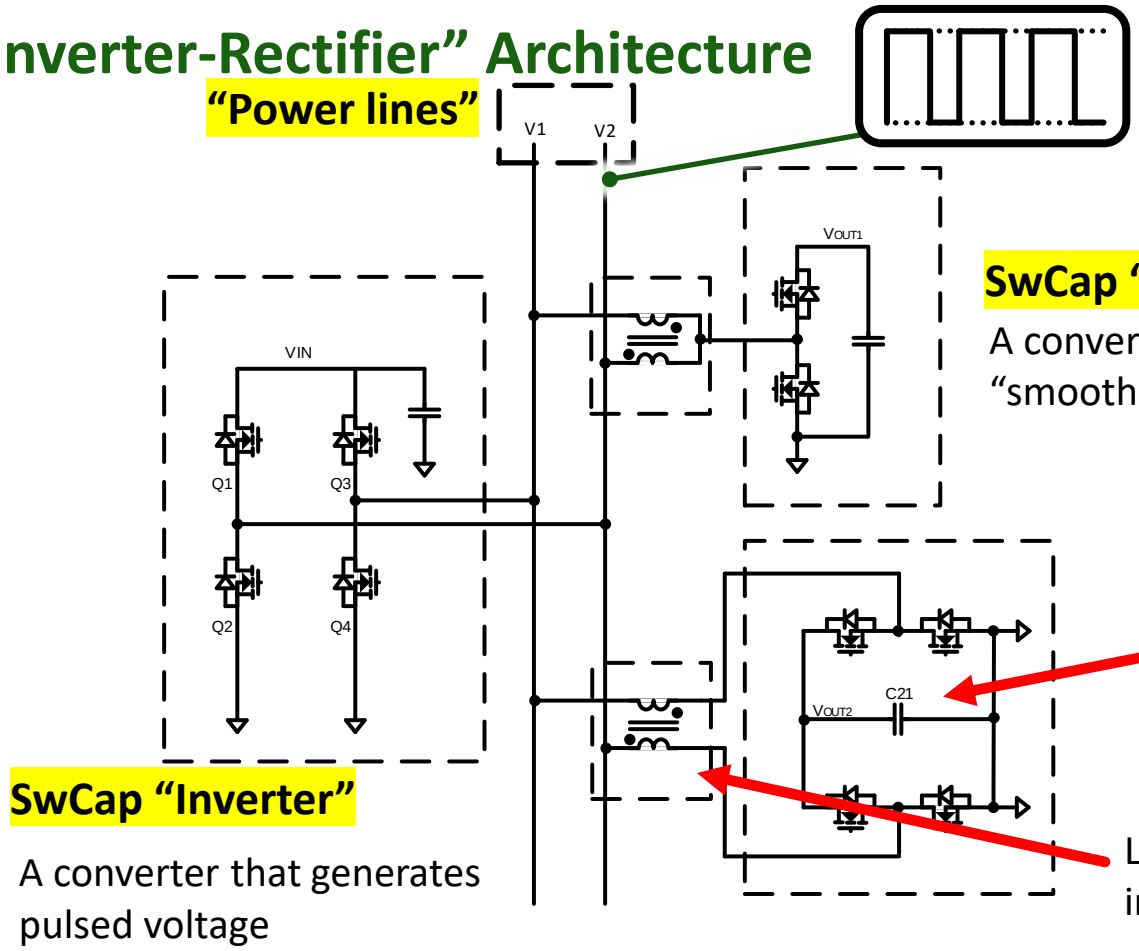




- High efficiency soft-charged front end generating multiple interleaved, unregulated alternating bus voltages
- Mix-and-match output stages with different switching frequencies and output voltages
- No bus capacitors, multiple **inductor-link rails**

on-chip

“Inverter-Rectifier” Architecture



SwCap “Rectifier”

A converter that “smooths” pulsed voltage

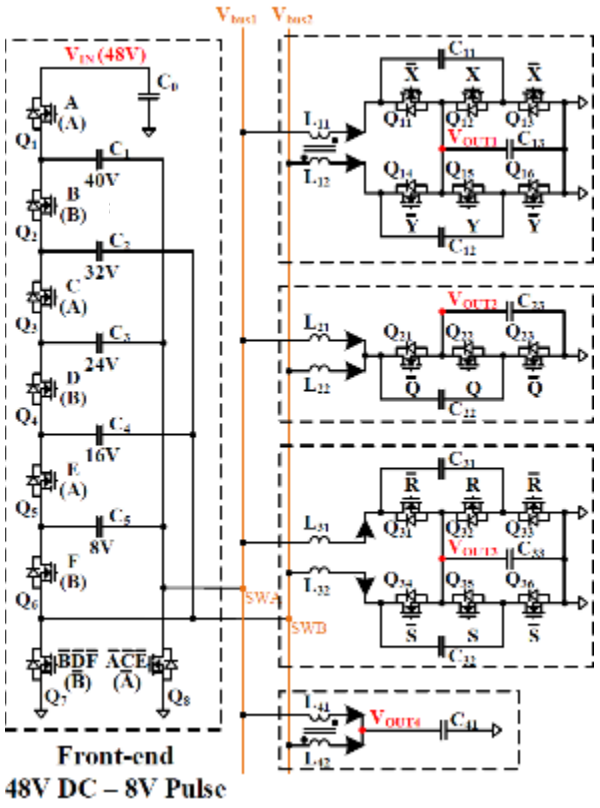
Leverage high density capacitors close to Chiplet or on-chip

SwCap “Inverter”

A converter that generates pulsed voltage

Leverage current smoothing inductor off-chip

Example Implementation of the Inductor Link Architecture



- Front-end: Dickson-like step-down architecture
- Back-end: Inductor-link switched cap rectifier

Front end:

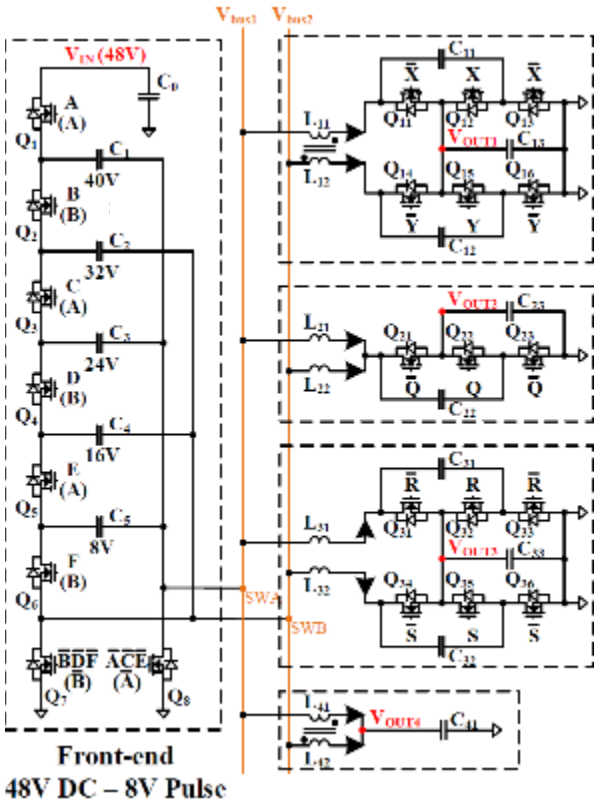
- Efficiently convert 48V into pulsed 8V rail voltage
- Average rail voltage between 0V and 8V

Back end:

- Convert pulsed rail voltage into regulated dc voltage
- Output voltage between 0V and average rail voltage

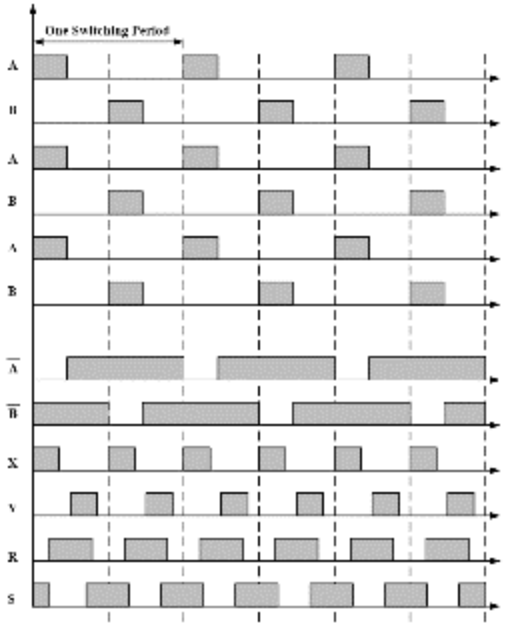
Front end and back end separately controlled and separated regulated. One front-end can be loaded by multiple back-ends with different power handling capability.

Example Implementation of the Inductor Link Architecture

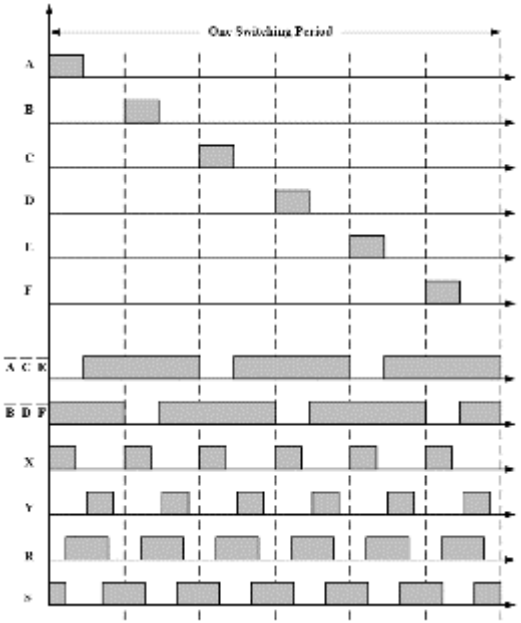


Multiple switching implementations are possible

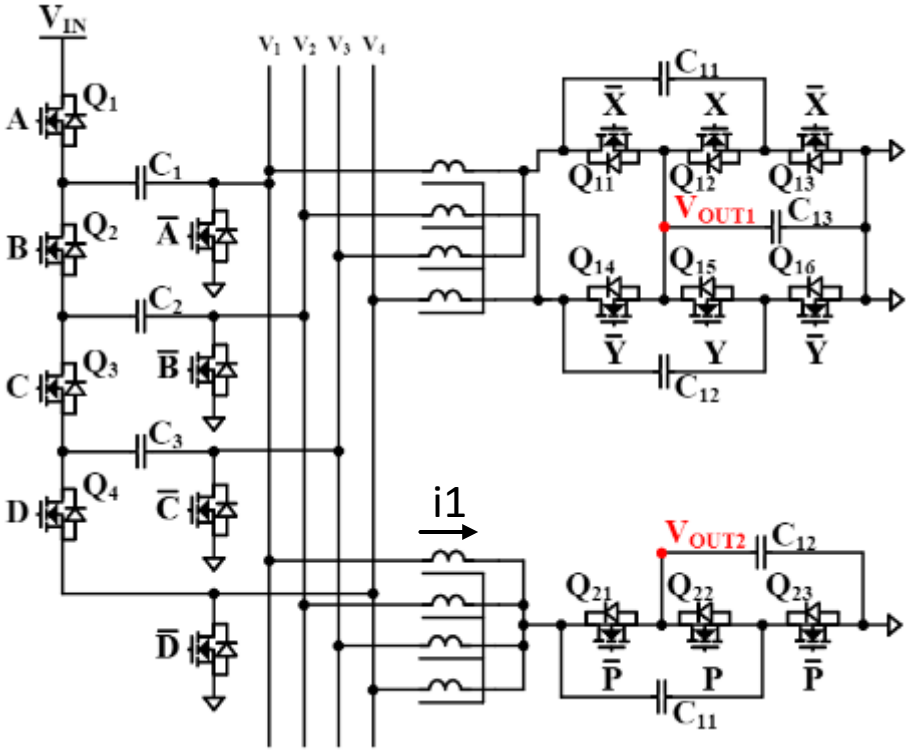
Hard-charging

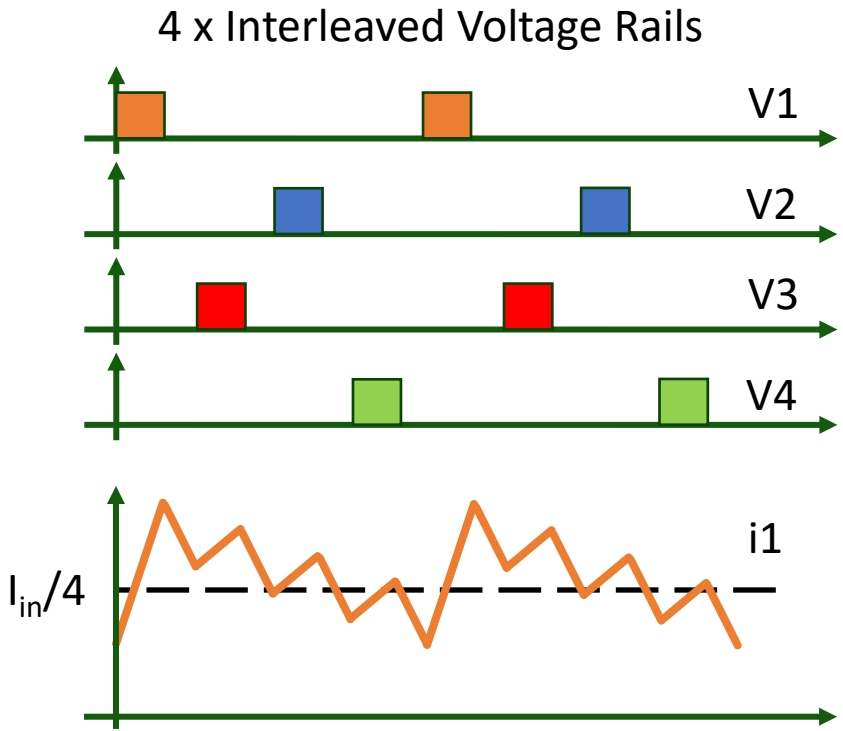


Soft-charging



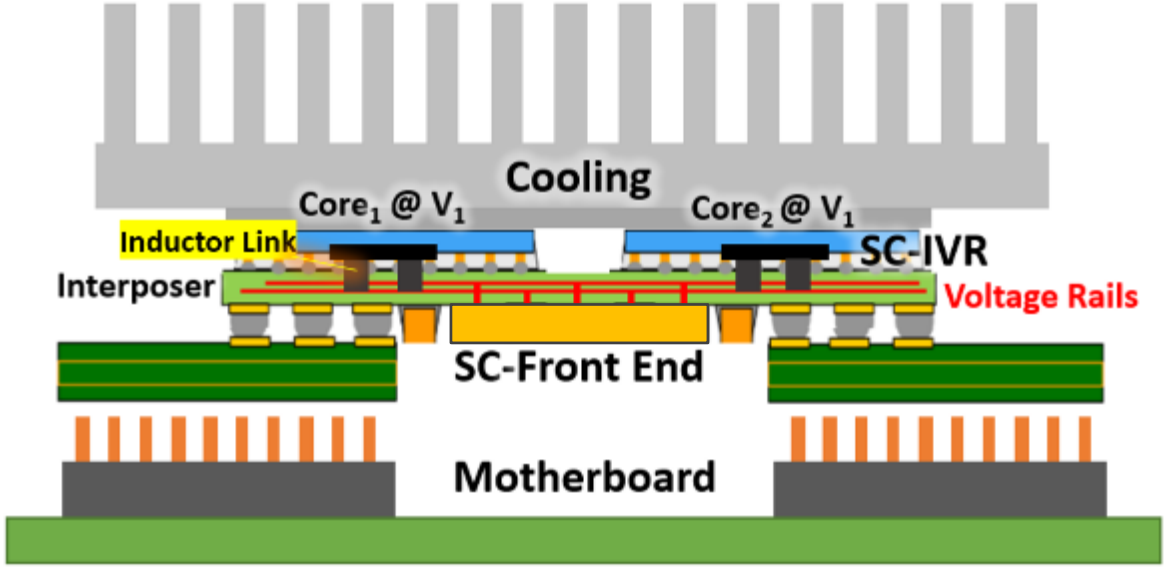
Multi-Rail Implementation with Full Soft Charging

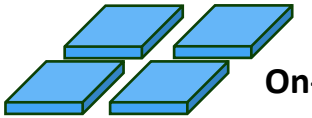




- Fully soft-charged front end, higher power delivery capability, smaller current ripple

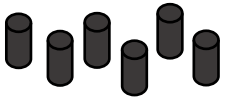
3D Packaging Concept for the Inductor-Link Architecture





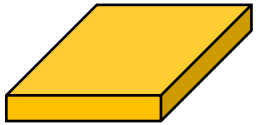
Module #3

On-Chip SwCap Backend



Module #2

Vertical Inductor Link



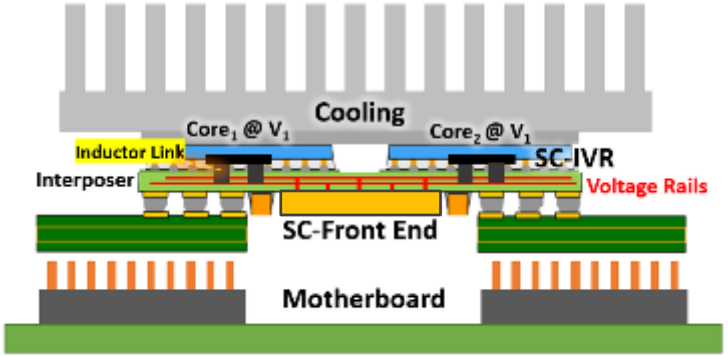
Module #1

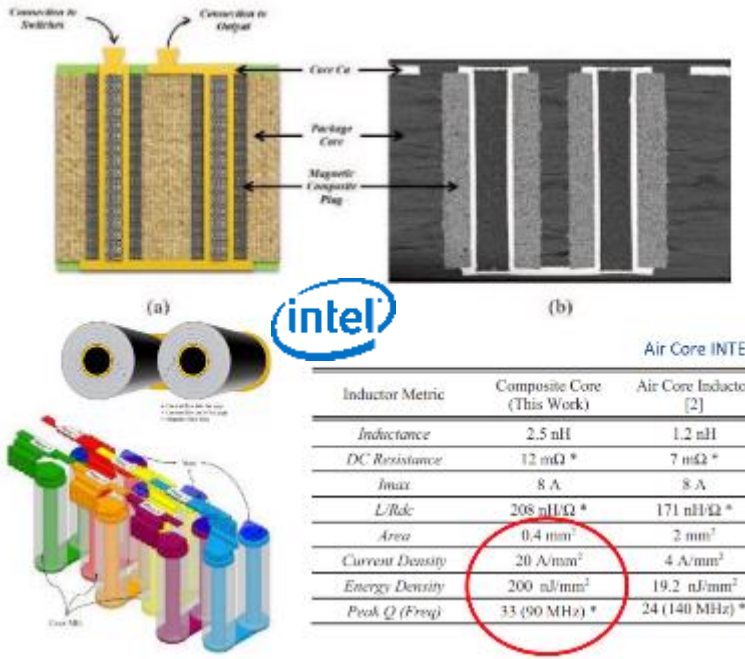
SwCap Front-End

Requirements 48V-1V >1A/mm^2 <7 mm height 500A~1000A 5A/ns 90%

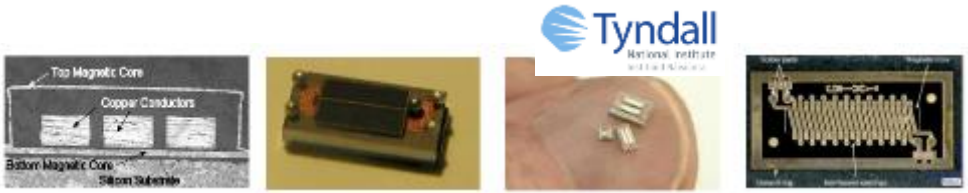
Conversion Ratio	*Area Density*	*Power/Signal/Thermal*	*Transient*	*Efficiency*

On-Chip / In-substrate Coupled Inductor





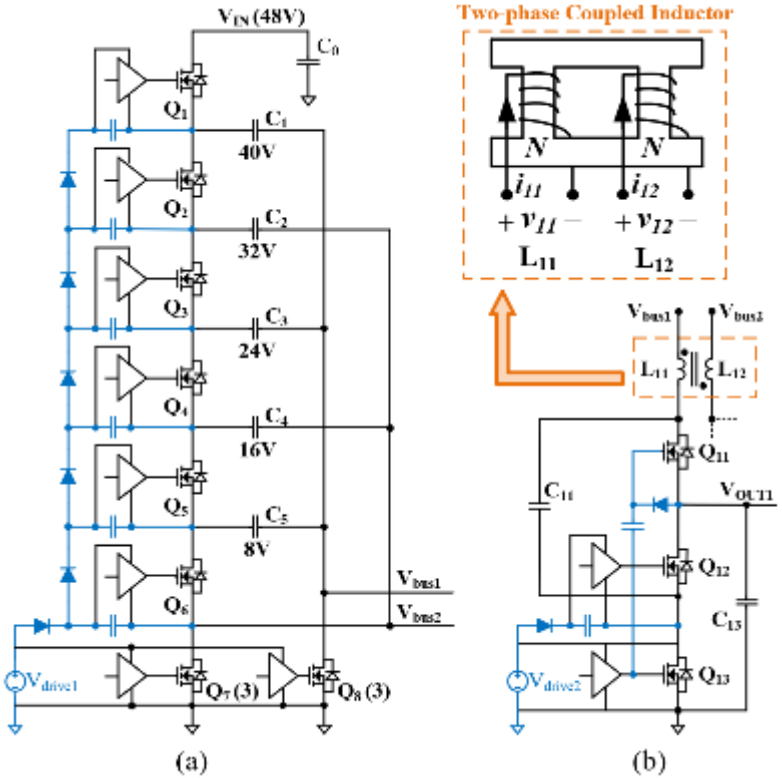
Inductor Metric	Composite Core (This Work)	Air Core Inductor [2]
Inductance	2.5 nH	1.2 nH
DC Resistance	12 mΩ *	7 mΩ *
Imax	8 A	8 A
L/Rdc	208 nH/Ω *	171 nH/Ω *
Area	0.4 mm^2	2 mm^2
Current Density	20 A/mm^2	4 A/mm^2
Energy Density	200 nJ/mm^2	19.2 nJ/mm^2
Peak Q (Freq)	33 (90 MHz) *	24 (140 MHz) *



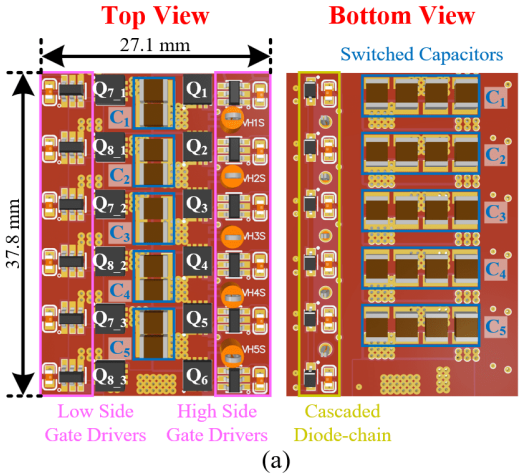
- Bharath, K., Radhakrishnan, K., Hill, M. J., Chatterjee, P., Hariri, H., Venkataraman, S., . . . Srinivasan, S. (2021, 1 June-4 July 2021). Integrated Voltage Regulator Efficiency Improvement using Coaxial Magnetic Composite Core Inductors. Paper presented at the 2021 IEEE 71st Electronic Components and Technology Conference (ECTC).

Prototype System Implementation

Cascaded Boot-strap Gate Drive Circuits

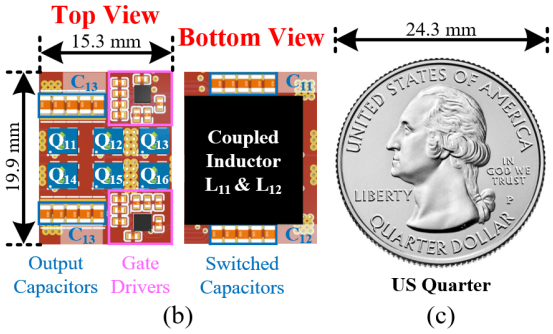


Front-End

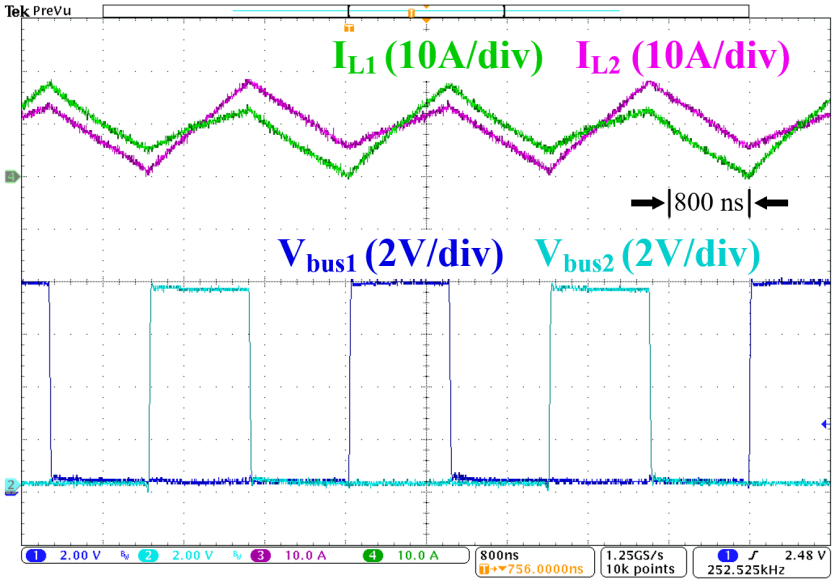


Back-End

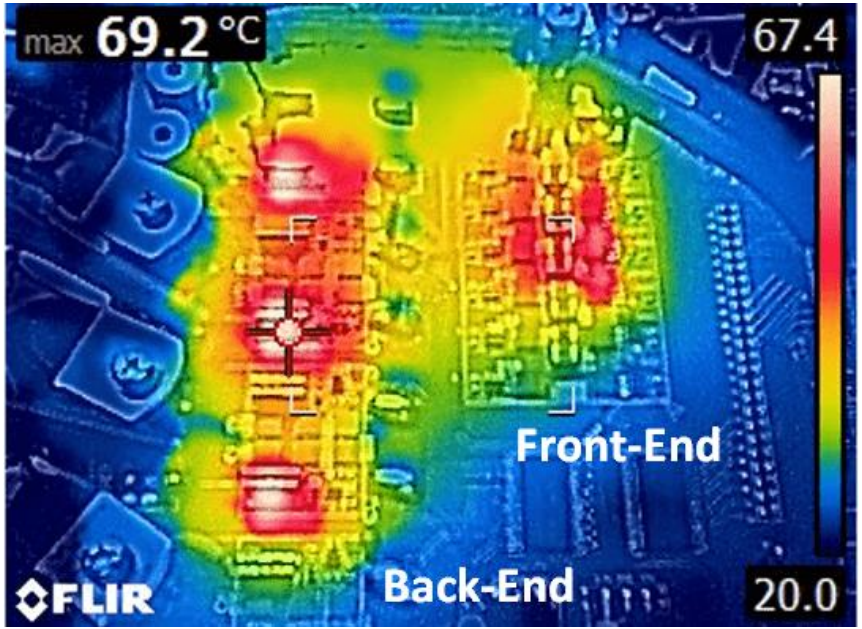
Eaton CL1208 Coupled Inductor



Operation Waveforms



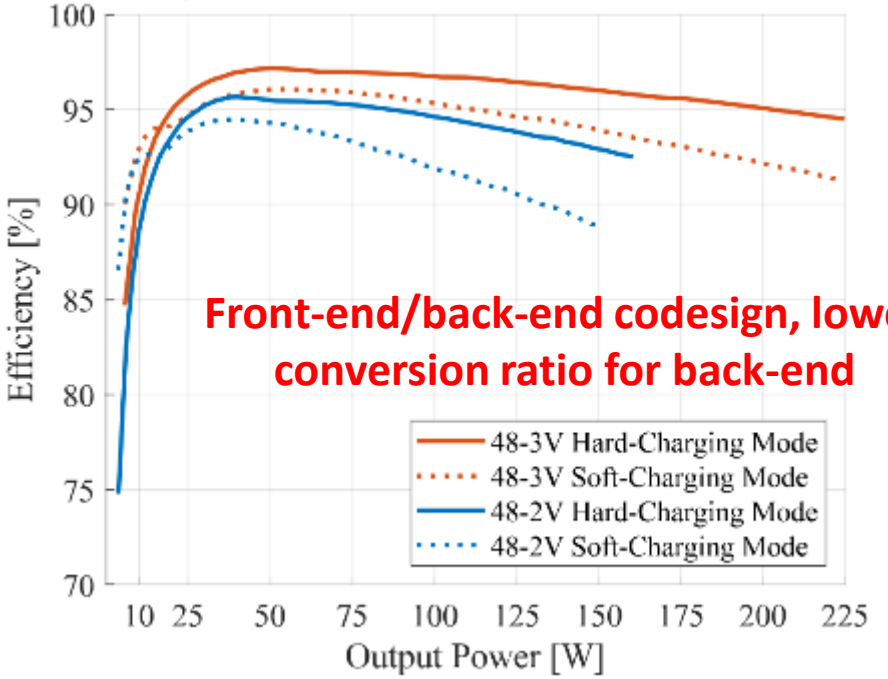
48 V to 2 V average bus voltage, 252.5 kHz front-end frequency with hard-charging pattern



48-V to 1.3-V/140A in hard-charging mode with 72-ft^3/min air flow from the bottom.

Measured Efficiency

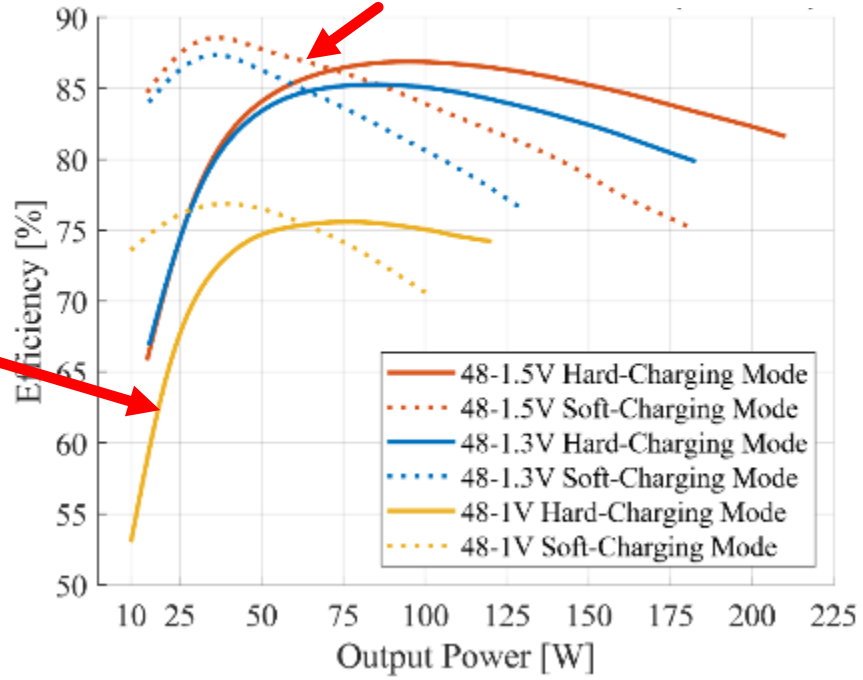
High efficiency front-end inverter stage:



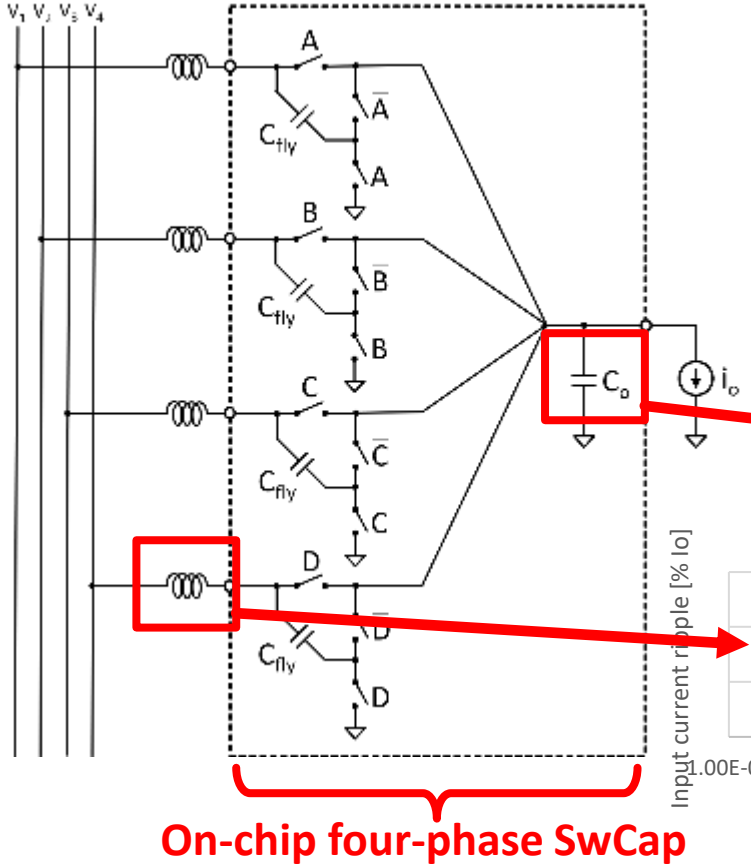
Front-end/back-end codesign, lower conversion ratio for back-end

Full architecture efficiency:

Soft-charging for light load



Design Considerations of the Switch-Cap Rectifier

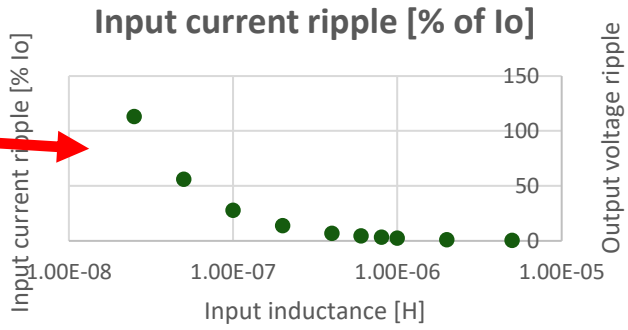


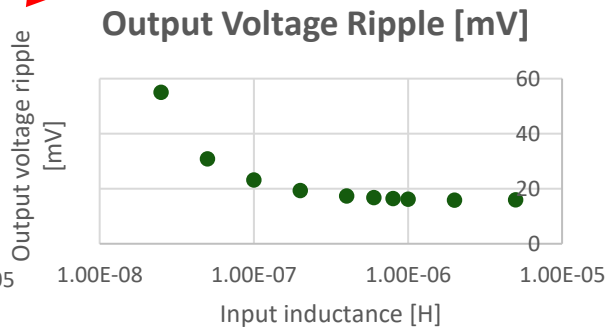
On-chip four-phase SwCap

Input: 8V pulsed at 22.5% duty cycle, 250~1000 kHz
Output: 1V to 1.5V (20% to 80% duty cycle)
Target: 10mV output ripple at 50 A output

First and second stage codesign:

- First stage provides unregulated pulsed voltage, but current ripple should be small
- Min. bus voltage for higher second stage duty cycle



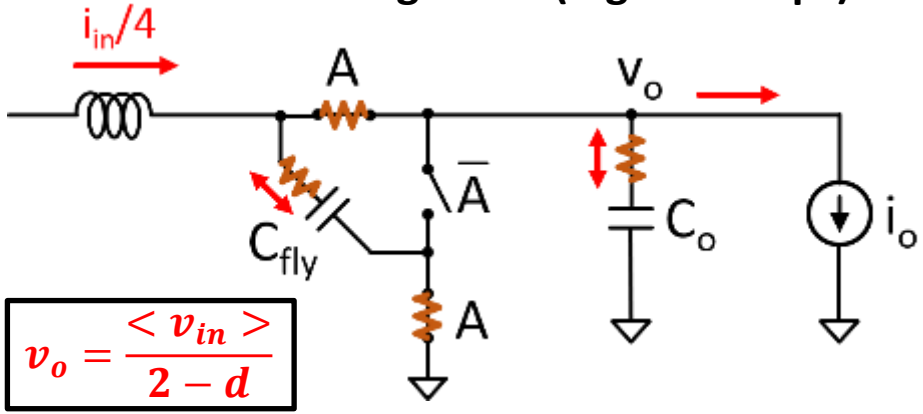


Design Considerations of the Switch-Cap Rectifier

Capacitors determine loss and v_o ripple

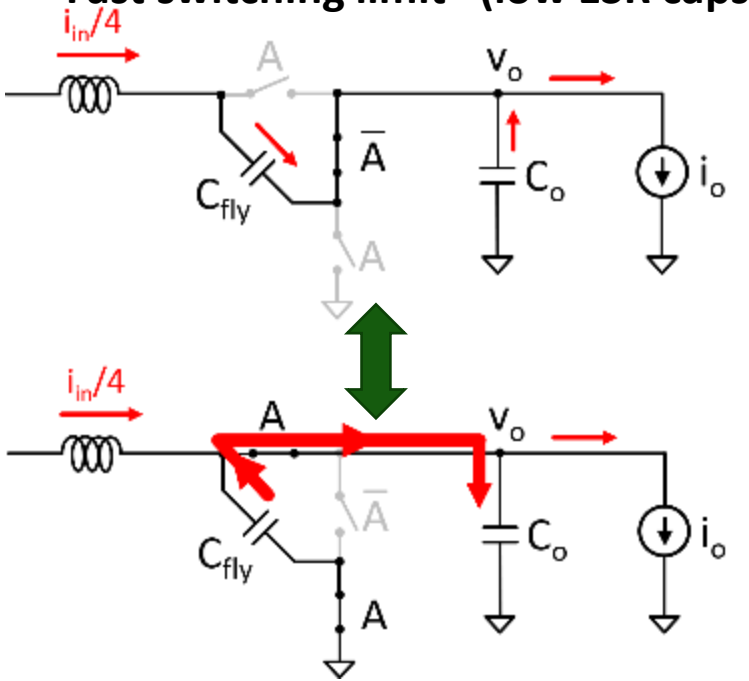
- Off-chip caps: ESR @ fsw = 10 MHz >> switch $R_{ds(on)}$
- If caps have low ESR (e.g. on-chip), charge sharing dominates loss and ripple

"Slow switching limit" (high ESR caps)



$$v_o = \frac{< v_{in} >}{2 - d}$$

"Fast switching limit" (low ESR caps)

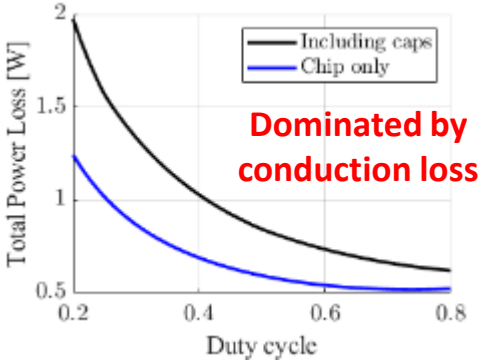


M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," in *IEEE Transactions on Power Electronics*

Design Considerations of the Switch-Cap Rectifier

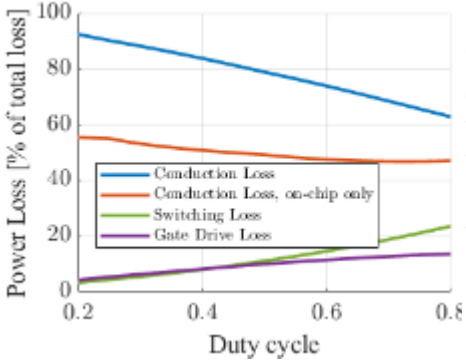
PRINCETON UNIVERSITY

Total Predicted Loss

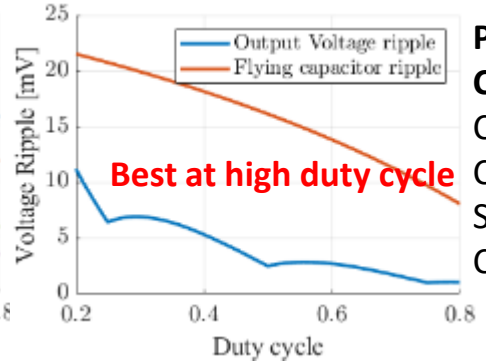


Dominated by conduction loss

Loss Breakdown

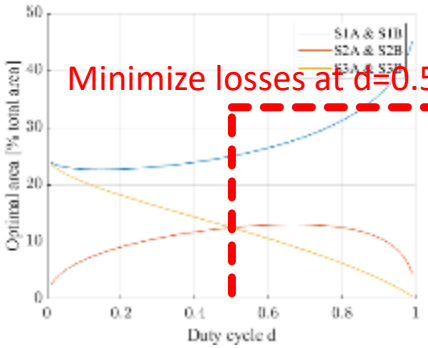


Predicted Ripple

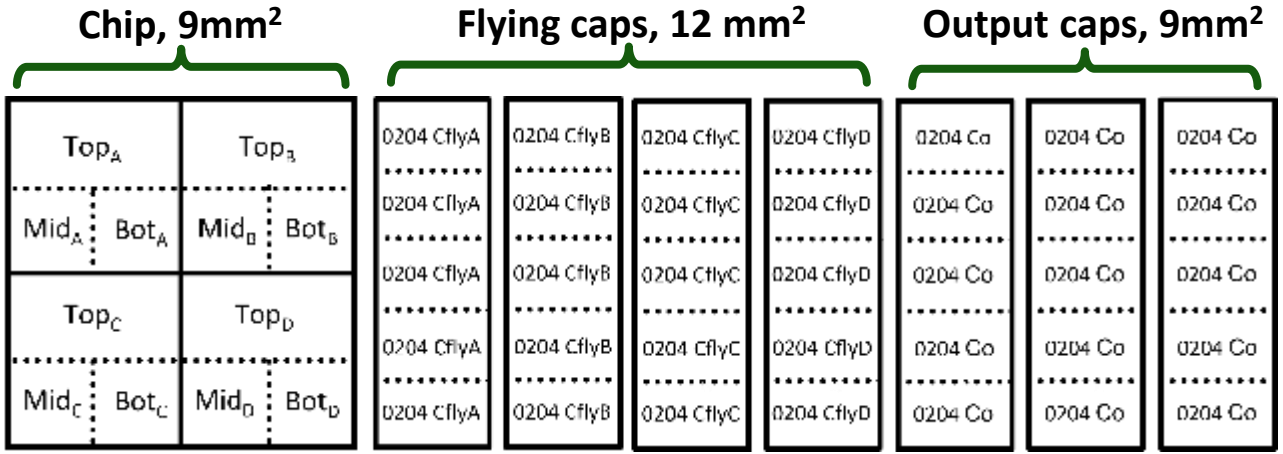


Best at high duty cycle

Process: 180 nm, 1.8V NMOS
Chip size: 3mm * 3mm
C_{fly}(per-phase) = 26 uF
C_o(total) = 47 uF
Switch $R_{ds(on)}$= 0.5/1 mΩ
Capacitor ESR = 0.9/0.3 mΩ



Minimize losses at d=0.5



Conclusion

48V Chiplet power delivery architecture with inductor link and multiple outputs