3D Power Delivery for High Performance Processors

3D PEIM – February 2023

FERRIC INC.

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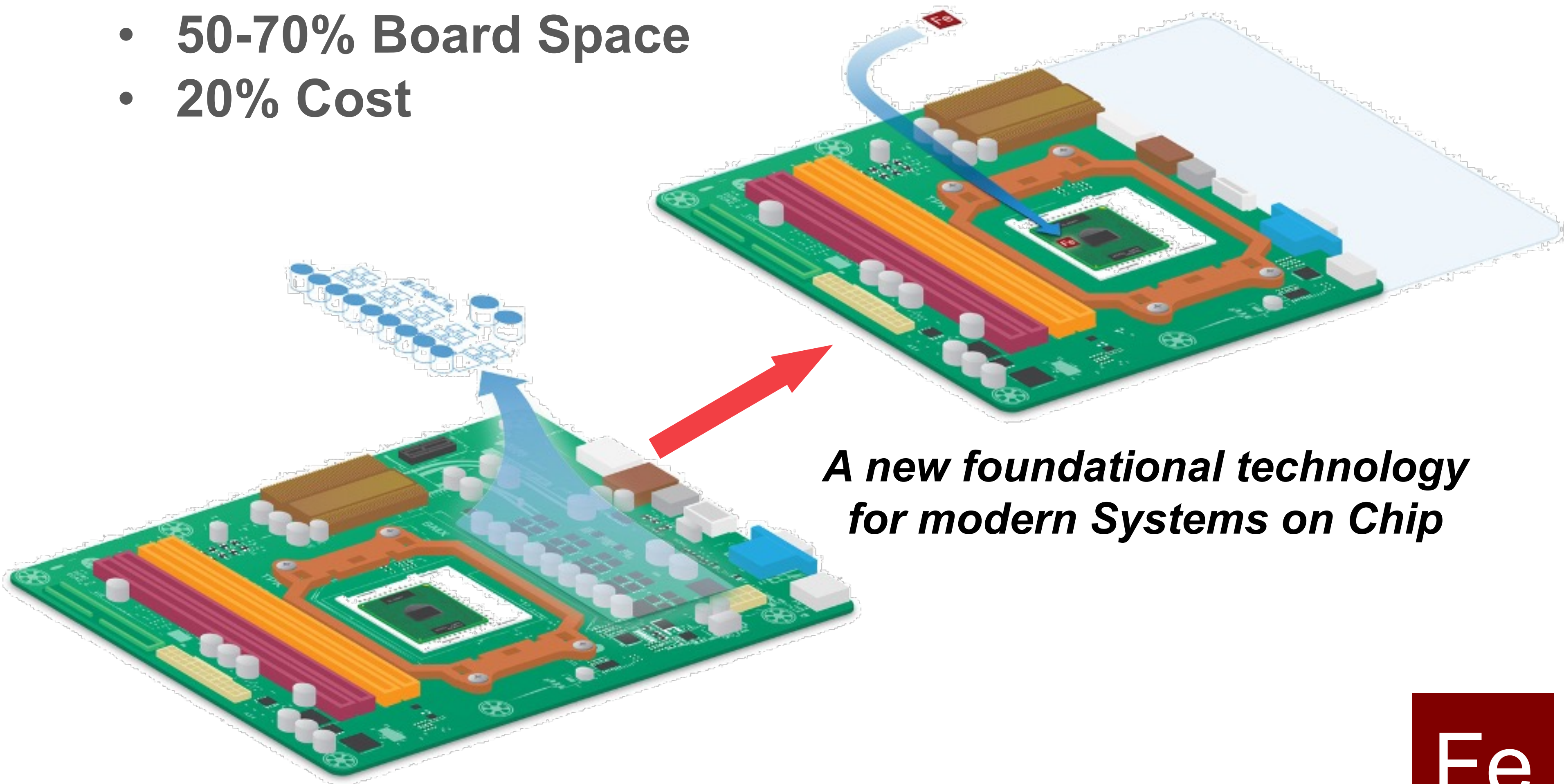
NEXT GEN ELECTRONICS REQUIRE
NEXT GEN POWER SYSTEMS

Integrated Power Converters enable savings…

- 20-50% Power
- 50-70% Board Space
- 20% Cost



A new foundational technology for modern Systems on Chip

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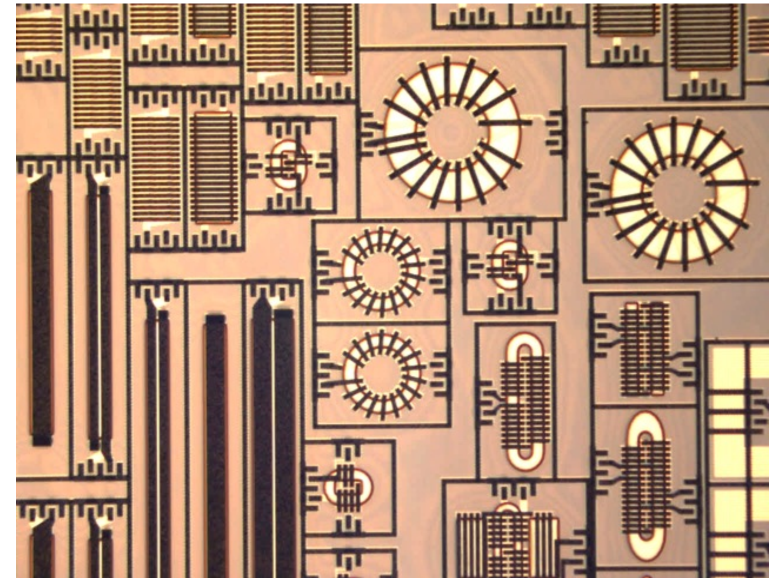
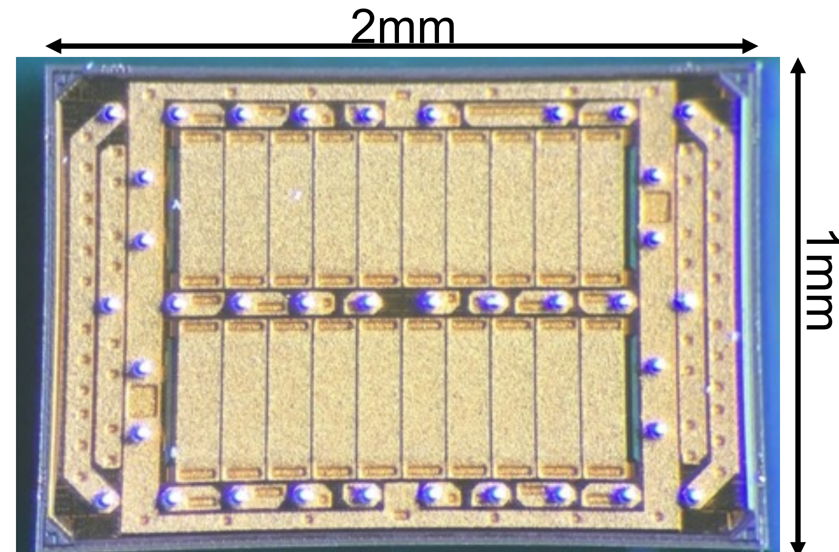
FERRIC IVR TECHNOLOGY

- **Thin-Film Magnetic Components**
  - Inductance density
    - > 300nH/mm², > 8,500nH/mm³
  - Current density > 12A/mm²
  - DC Resistance < 100mΩ
  - Magnetic Coupling k > 0.9
  - Ferric Technology fabricated by TSMC



Ferric Magnetic Components

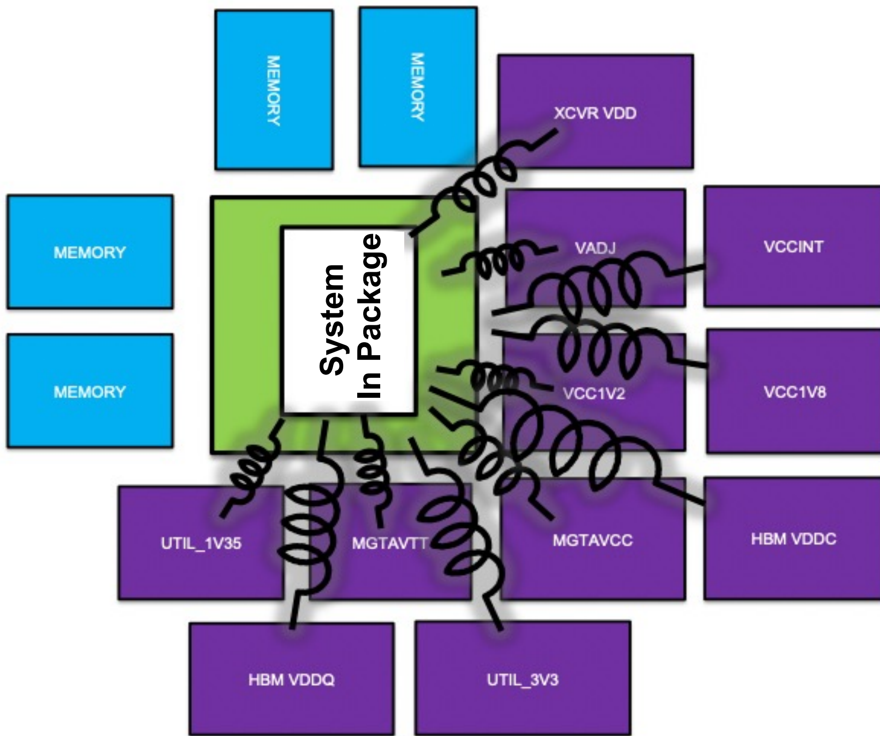
- **DC-DC Converter Chiplets**
  - High switching frequency > 100MHz
  - High bandwidth controller > 10MHz
  - Optimization for high efficiency >90%
  - Optimization for high density ~2A/mm²



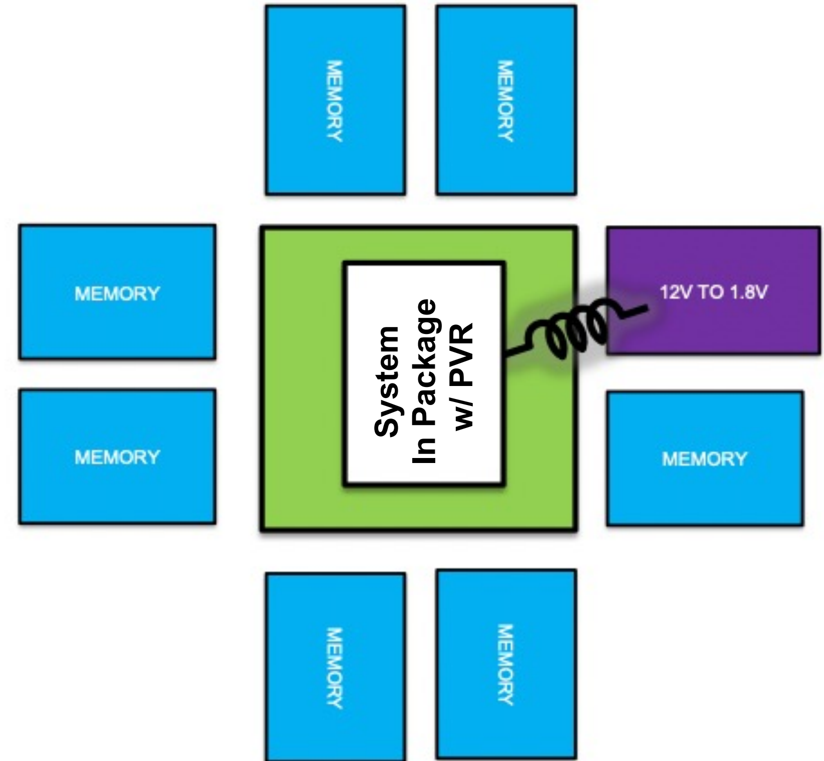
Ferric Power Converter Chiplet

Integration Reduces System Complexity

Conventional SiP



SiP with PVR



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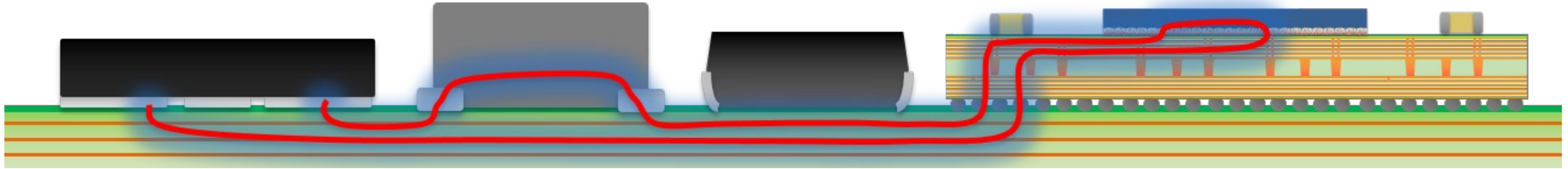
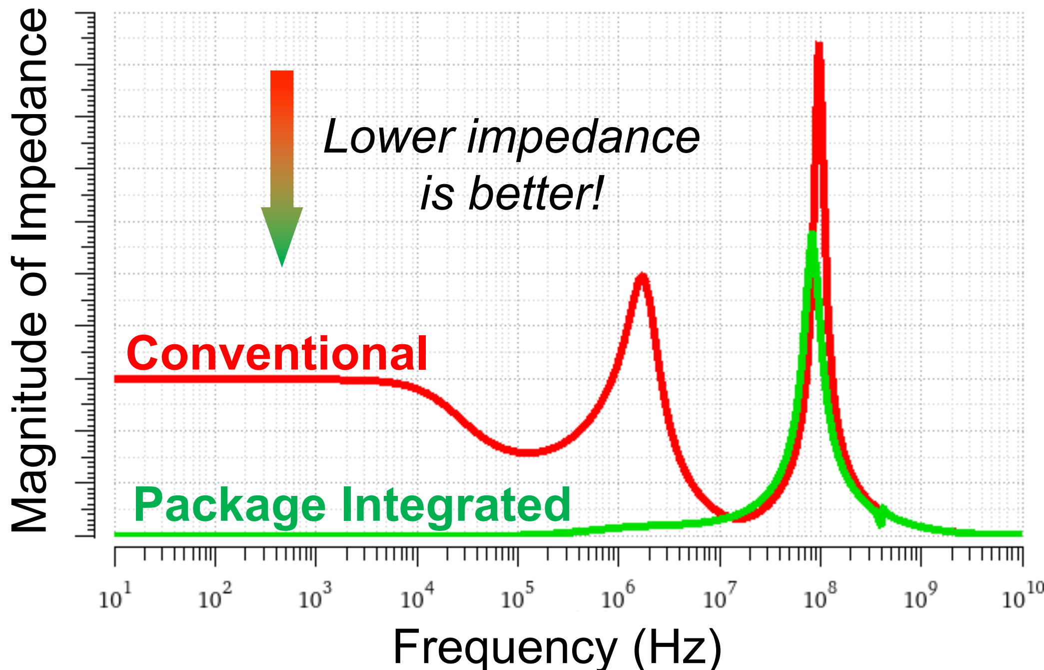
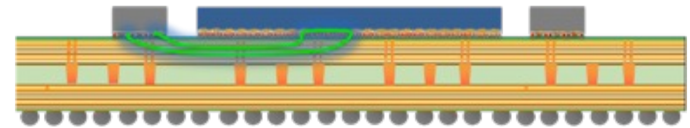
2D Package Integrated Voltage Regulator



Conventional Power Delivery Network (PDN)

Integrated Power Delivery Network (PDN)





Smaller loop inductance

Less bulk capacitance

Higher feedback bandwidth

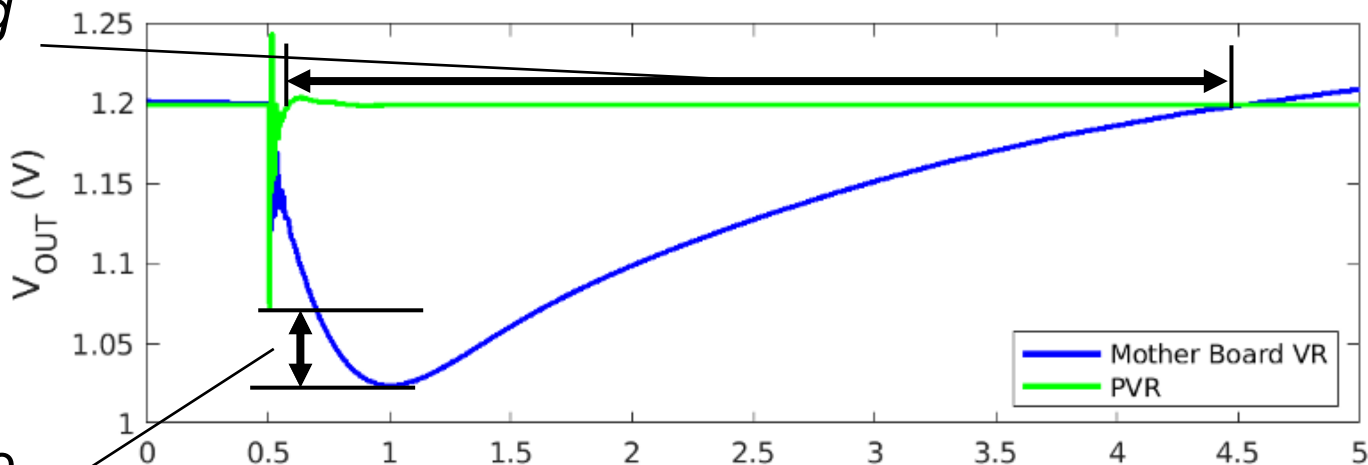
Fewer parasitics

Less impedance overall

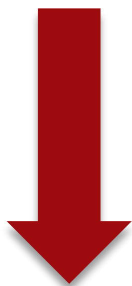
PACKAGE VR *Power Integrity Comparison*

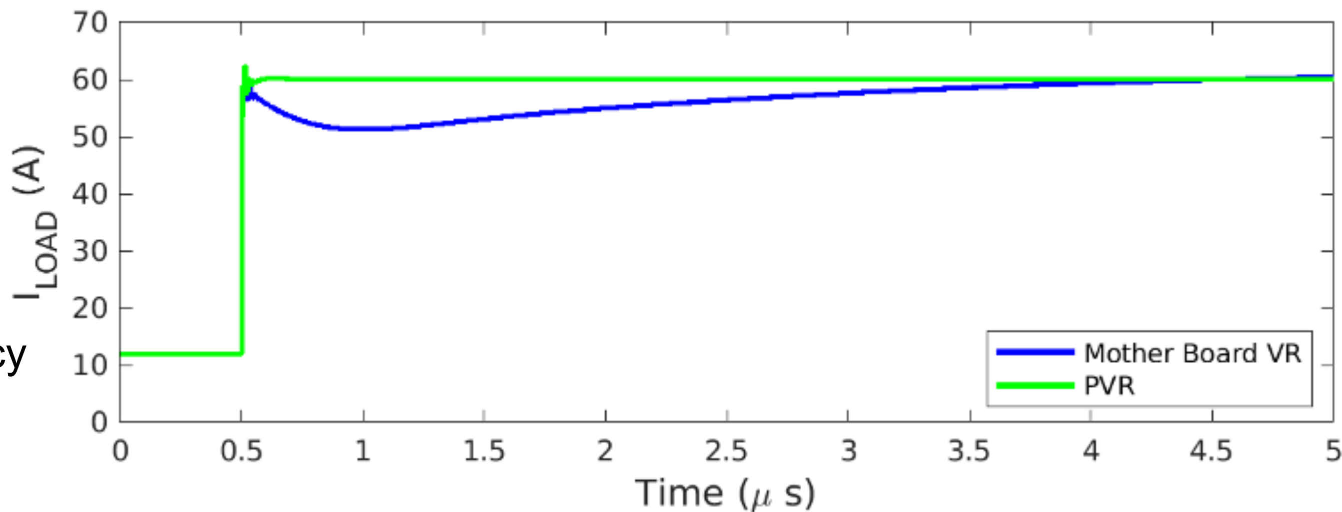
Load Current Step Response for Mother Board VR vs PVR

Reduce settling time by 40x



Reduce voltage droop by 28%





- Increased frequency
- Power savings

PACKAGE VR Performance Gains

Integrated Power Converters enable >5% increase in clock frequency at constant supply voltage

Supply Voltage

Safe Operation with Incumbent power solution

Safe Operation with IVR

Data Faults

Clock Frequency

Load-line reduces need for supply margins even with incumbent solution

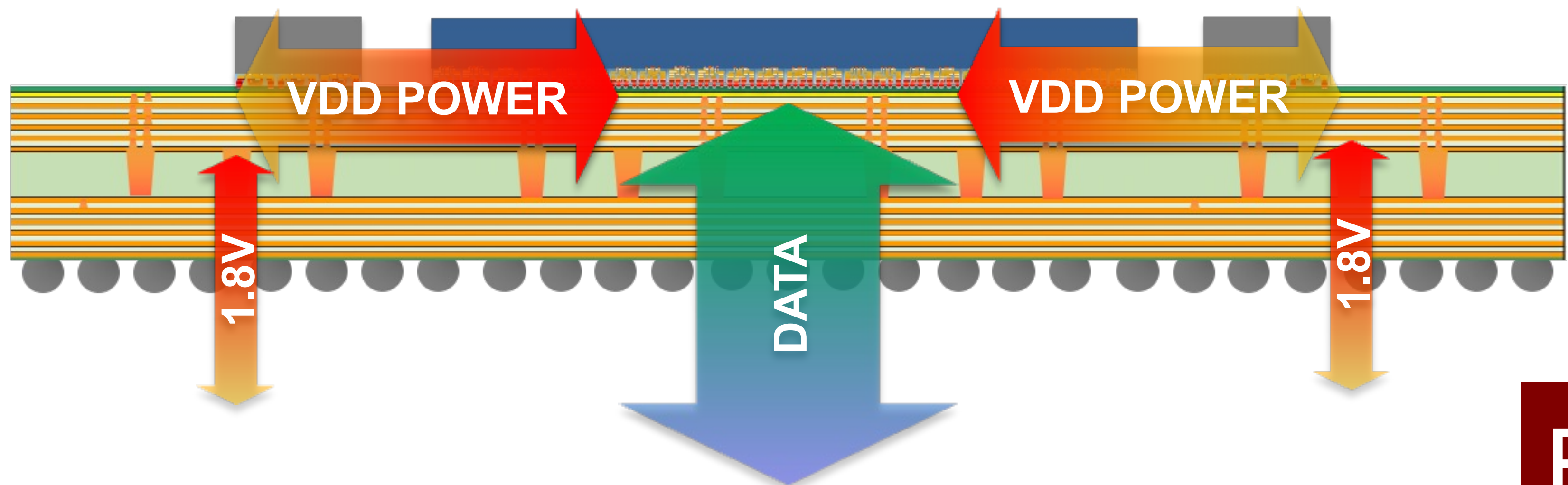
Required Supply Voltage Margins for transient error are reduced significantly with PVR

PACKAGE VR Power & Data Bottlenecks

- Package Voltage Regulators reduce power supply current at Package-to-board interface by ~3x, allowing:

  ~2x higher signal bandwidth or ~40% reduction in pin count

- New bottlenecks for in-package power delivery must be avoided
- Power & Data bottlenecks can still occur at chip-to-package interface



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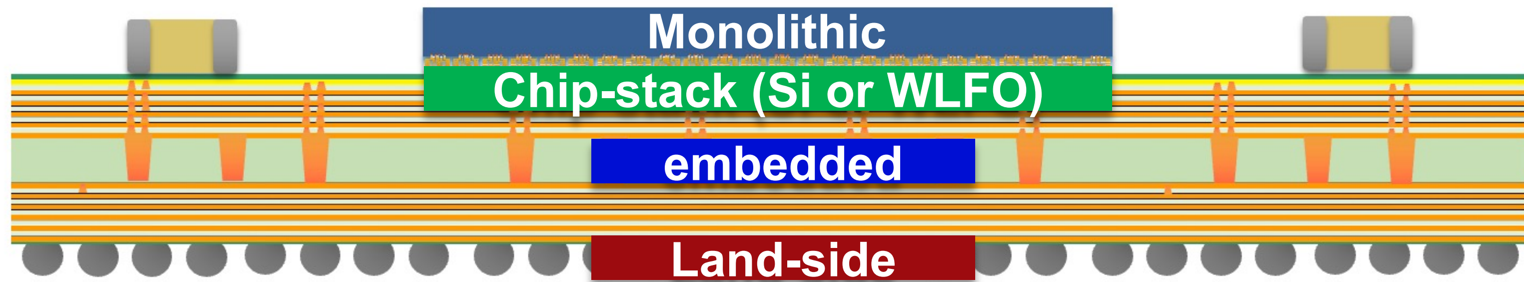
3D Power Delivery Implementations

3D Power Delivery is a promising solution to bottles arising from 2D IVR implementation, but where do we put the IVR?



Monolithic – VR implemented director on processor substrate

Chip-Stack – VR implemented on an active silicon interposer or WLFO interposer

Embedded – VR embedded into core of processor substrate under processor

Land-side – VR attached to surface of package substrate opposite the processor die

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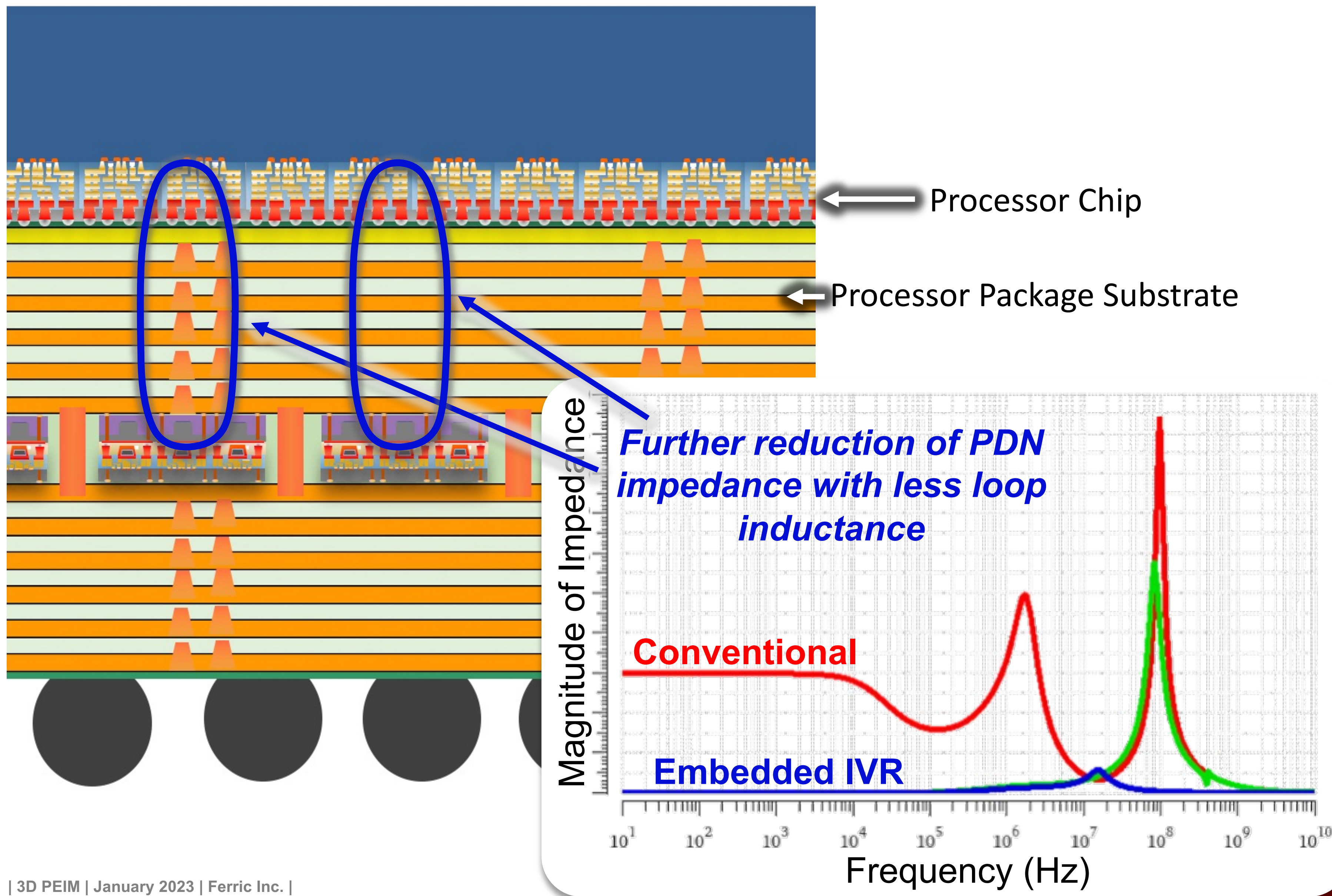
Processor with Organic Substrate Embedded PVRs



3D Power Deliver ***Performance Gains***

3D power delivery approaches further improve reduce processor PDN impedance and enable further reduction in supply voltage margins and corresponding wasted power

Supply Voltage

Safe Operation with Incumbent power solution

Die-Side (2D), Land-side

Monolithic, Chip-Stack, Embedded

Data Faults

Clock Frequency

Load-line reduces need for supply margins even with incumbent solution

Better transient response for 3D converters enables reduced supply voltage margin

Requirements for 3D Power Delivery

- **Functional**
- **Density**
  - – Current density (area) of VR must match or exceed current density of load: >2A/mm^2
  - – Profile of VR must fit package implementation: 20um – 0.8mm
- **Thermal/Efficiency**
  - – VR must improve energy efficiency of processor
    - Reduction in PDN loss and Power Supply Margins > Conversion Loss
  - – VR *should* improve thermal budget of processor at max load
    - No PI benefit at max load because of load-line
    - opportunity to channel heat away from processor
    - duty cycling within thermal time-constant can still improve peak performance

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Comparison of 3D VR Implementations

Assuming all implementations capable of 90% conversion efficiency at max load

Monolithic – potentially best performance, but constraints on passives. Highest cost, cycle time and risk

Chip-Stack –Si implementation still has high cost, but enables heterogenous integration and design reuse, WLFO implementation allows chiplet reuse but TIV impedance may be prohibitive for some applications

Embedded – good balance of performance and cost, requires additional thermal design and high VR efficiency at max load but heat can be channeled to bottom of package

Land-side – most convenient of “3D” options, but higher PDN impedance from pkg core, requires thermal design conversion losses on landside, also blocks terminations on land-side

Die-side (2D) – most convenient, share thermal design with processor but still some thermal isolation, can have power and signal congestion

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PACKAGE VR Thermal Limit

2D, Embedded and Land-side approaches provide opportunity to channel heat from VR conversion losses away from processor, enabling potentially 10% better thermally limited performance relative to monolithic and chip-stack

FERRIC CHIPLET POWER CONVERTERS

Package Voltage Regulator

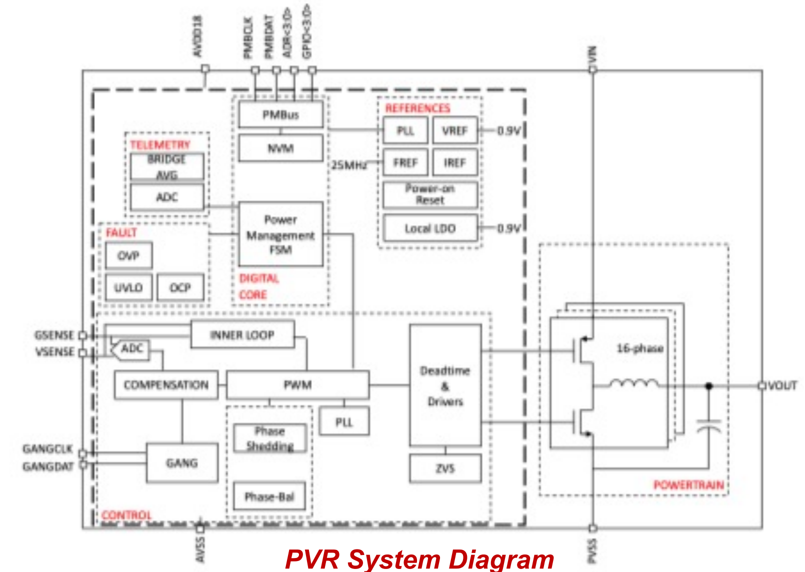
- **V_{IN} 1.6V-2.0V** :: **V_{OUT} 0.3V-1.5V** with **I_{OUT} 0-50A**
    - Integrated switches, inductors, controller, telemetry and references
- **Conversion efficiency ~90%**

- **Digital Feedback Controller**
    - 50MHz+ feedback control bandwidth
    - ±0.5% voltage accuracy
    - Up-to 18-phase DPWM with < 3mV resolution and < 200ps latency
    - Fast-Phase-Shedding inner control loop

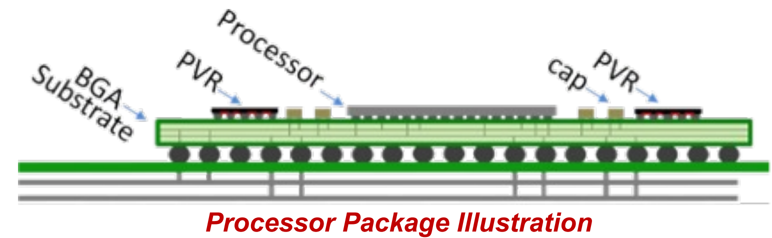
- **1MHz PMBus-Compliant Serial Interface**
    - Programmable V_{OUT}, F_{SW}, Compensation, Telemetry, Faults, etc.
    - Dynamic Voltage Scaling (DVS) bus for 200ns voltage transitions
    - Gang mode for 1-16 parallel chips (up to 480A)

Technology

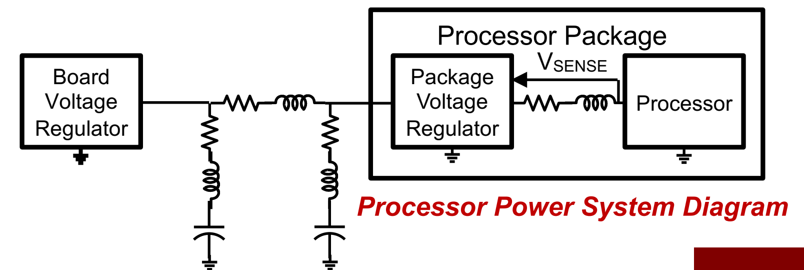
- **TSMC CMOS**
- **Ferric power inductors**
- **~2A/mm^2 chiplet current density**
- **Known-Good-Die (KGD) for package integration into FC-BGA/LGA or Si Interposer**



PVR System Diagram



Processor Package Illustration



Processor Power System Diagram

QUESTIONS?