

Insights from Microelectronic Packaging for Power Packaging Advancement

Matt Kelly, CTO & VP Technology Solutions IPC
3D PEIM International Symposium | Miami, Florida
Wednesday February 1, 2023

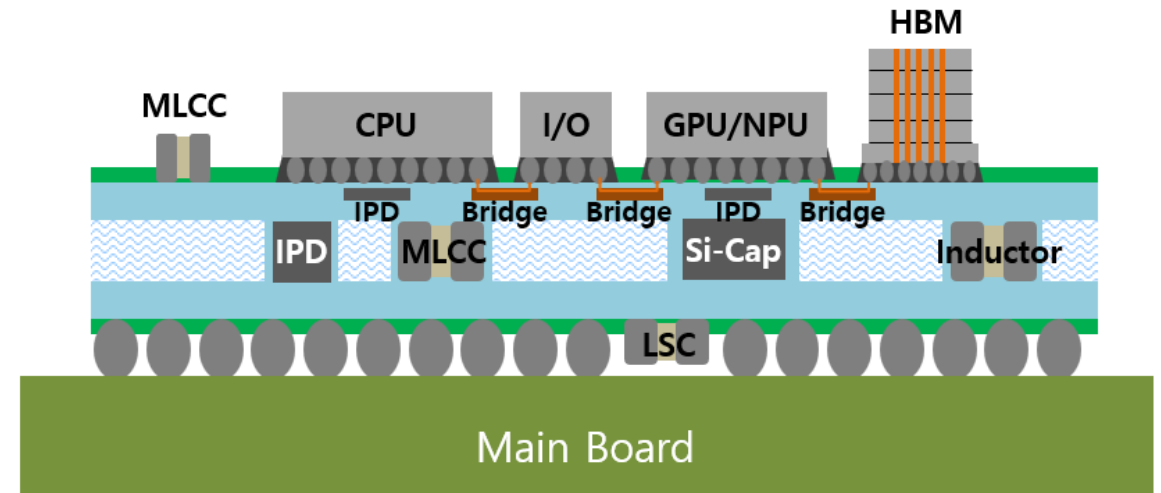


Image: R.Bae, Samsung-SEMCO, October 2022
IPC Advanced Packaging Symposium, Washington, DC

Accelerating Changes

→ North America, Europe, Asia

Everything follows Silicon

Silicon to Systems

Manufacturing Matters

Period of Massive Disruption

Rate, pace, disruptive technologies, shortages, sustainability, geo-political conflicts, inflation, resiliency, continuity of supply

→ Global & Regional Supply Chain model shifts



250+ Companies, 20+ Countries

**AN ANALYSIS OF THE NORTH AMERICAN
SEMICONDUCTOR AND ADVANCED
PACKAGING ECOSYSTEM**

Rebuilding U.S. Capabilities for the 21st Century



An IPC Summary Report — November 2021

- 115 pg. report. Data rich situation analysis
- **Influenced U.S. & EU policy, incentives programs, public-private investment**
- Dept Comm, Defense, NIST, NSC, IBAS
- EU Commission, Member State Parliaments
- **Need Advanced Packaging Ecosystem**



TOWARDS A ROBUST ADVANCED PACKAGING ECOSYSTEM

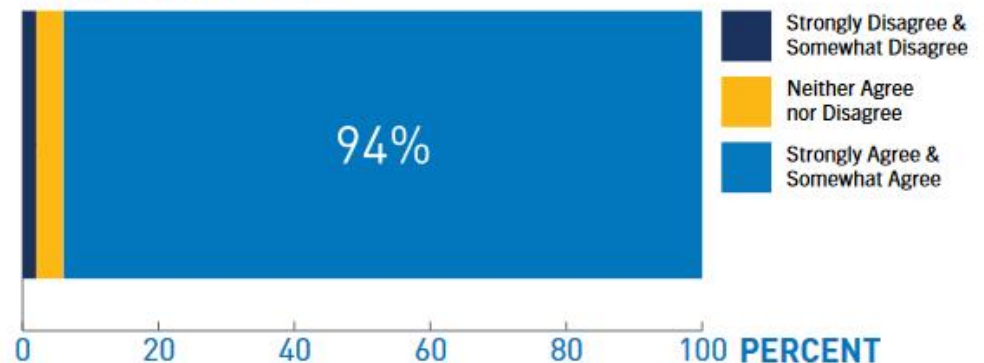
“Advanced Packaging is the New King”

Todd Younkin President & CEO
Semiconductor Research Corporation



with each new node requiring billions of dollars in investments. For example, at 7 nanometers, CMOS scaling is often prohibitively expensive. Most companies cannot carry the development and wafer costs, so they put together solutions using different technologies. Advanced packaging techniques, like SIP, enable companies to integrate multiple chips from different foundries within a single package.

IMPROVING THE PERFORMANCE OF SEMICONDUCTORS IS INCREASINGLY RELIANT ON ADVANCED PACKAGING



IPC ADVANCED PACKAGING SYMPOSIUM:

Building the IC-Substrate and Package Assembly Ecosystem

Kimpton Monaco Hotel, Washington DC October 11-12, 2022



Intent. Right people in the room – Full House

Target. Executive, Government, Industry, Academic Leaders

- Commercial and Defense Electronics

Stats & Highlights.

- 2 Days | 153 Attendees | 26 Speakers
- 4 Keynotes | 8 Sessions
- 100 Companies / Organizations
- 10 Countries – North America (90%), Europe, Asia
- 11 Supply Chain, Ecosystem Segments

Media. Washington Post, 007 IConnect

Feedback. Excellent, want more collaboration w/ IPC leadership



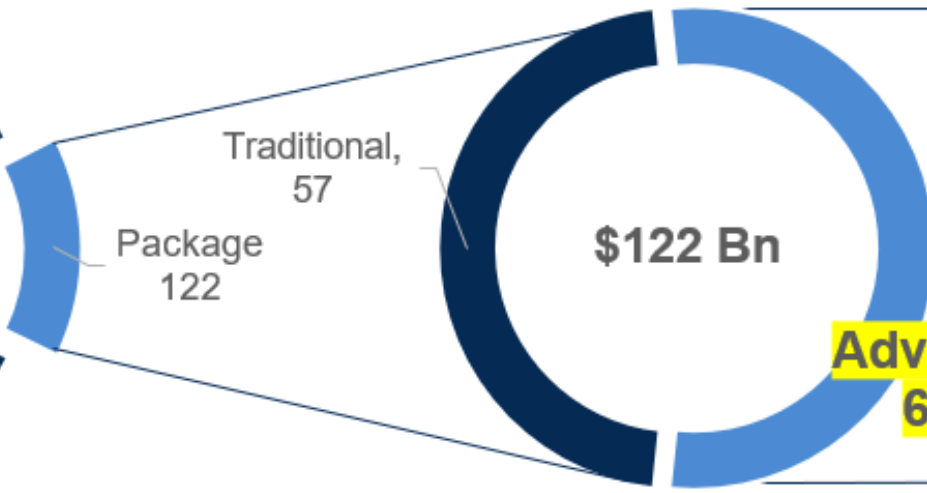
Semiconductor Market Outlook

2027

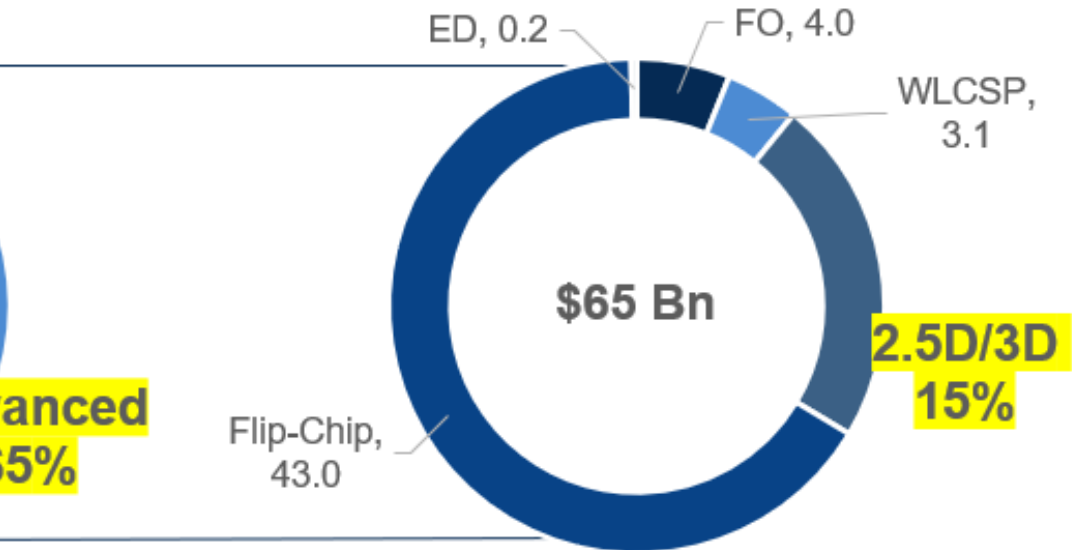
Semiconductor Revenues (\$Bn)



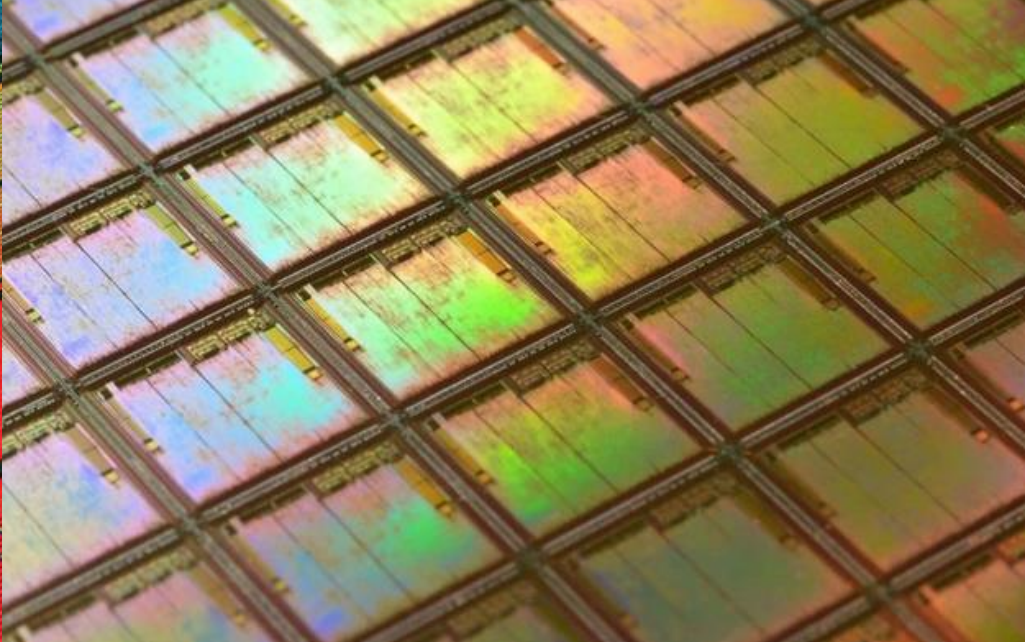
Packaging Revenues (\$Bn)



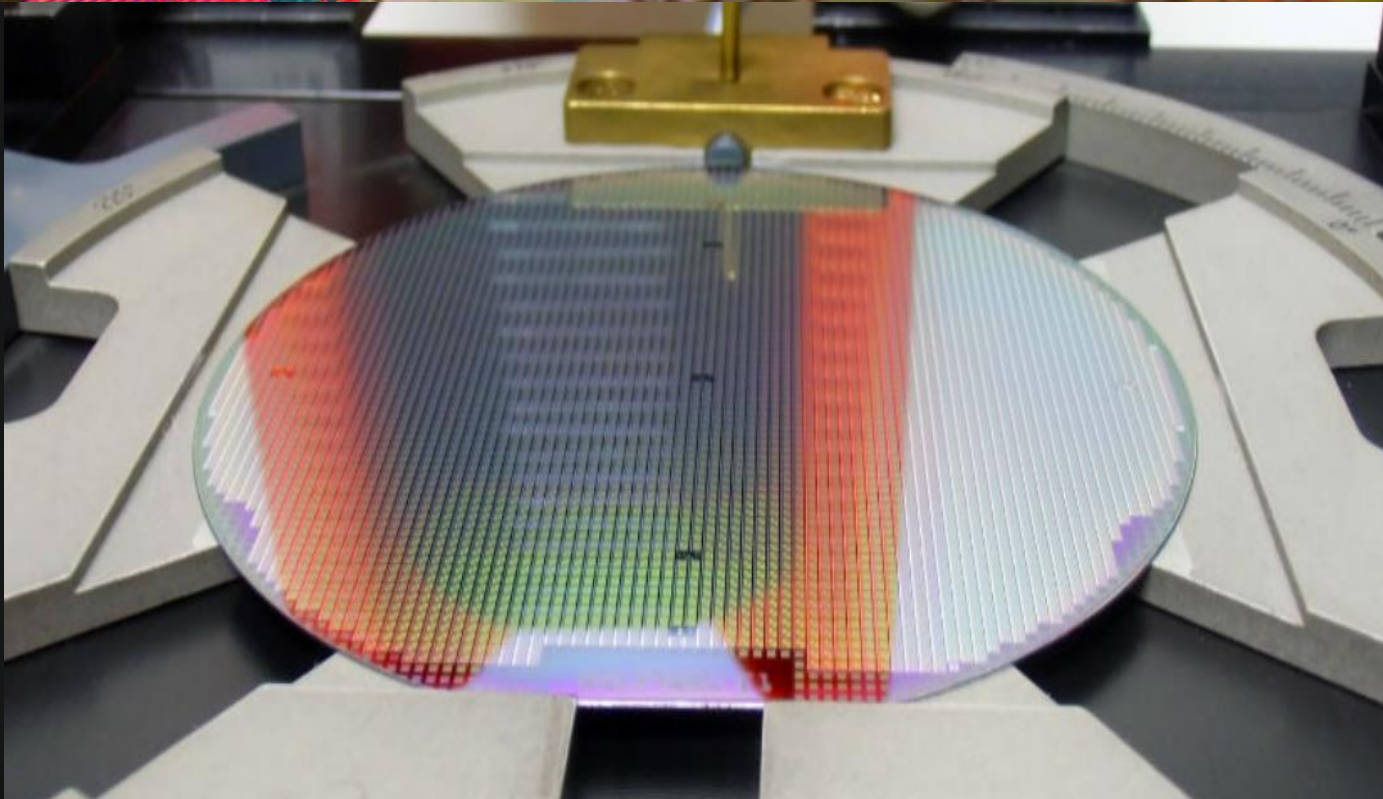
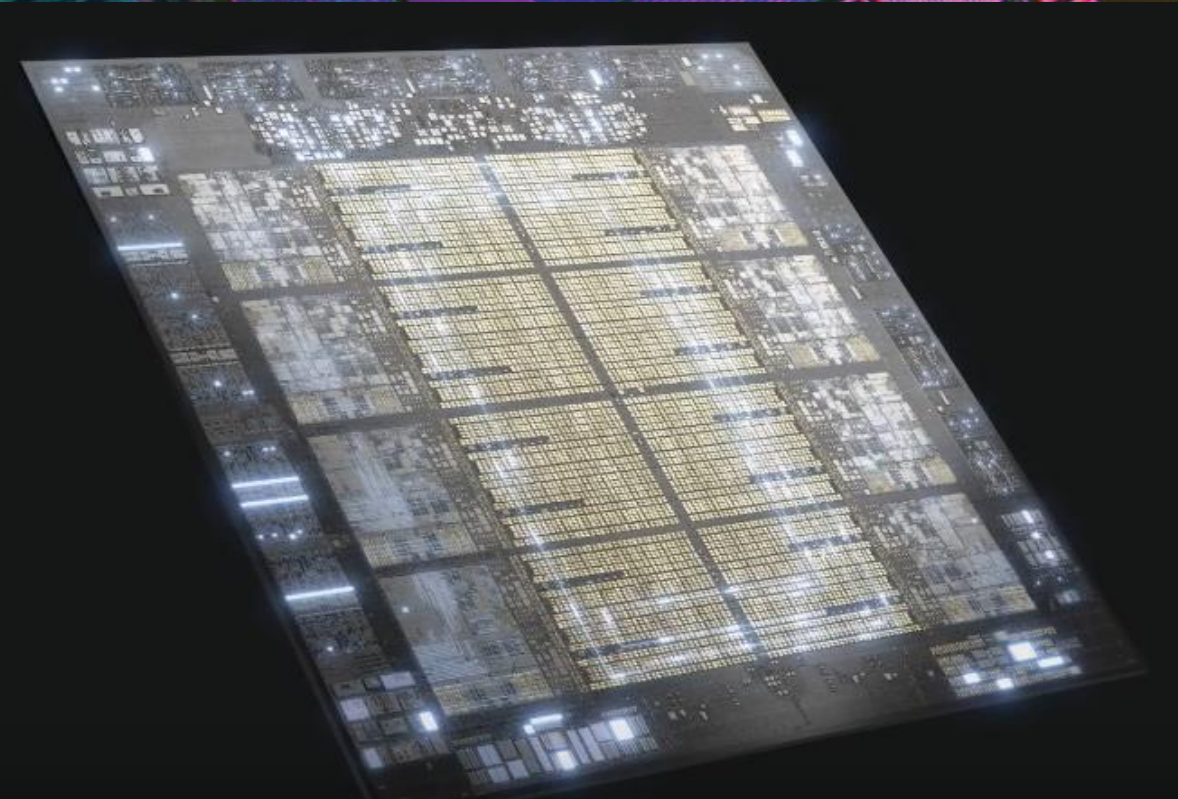
Advanced Packaging Revenues (\$Bn)



Source: AT&S October 2022
IPC Advanced Packaging Symposium, Washington, DC

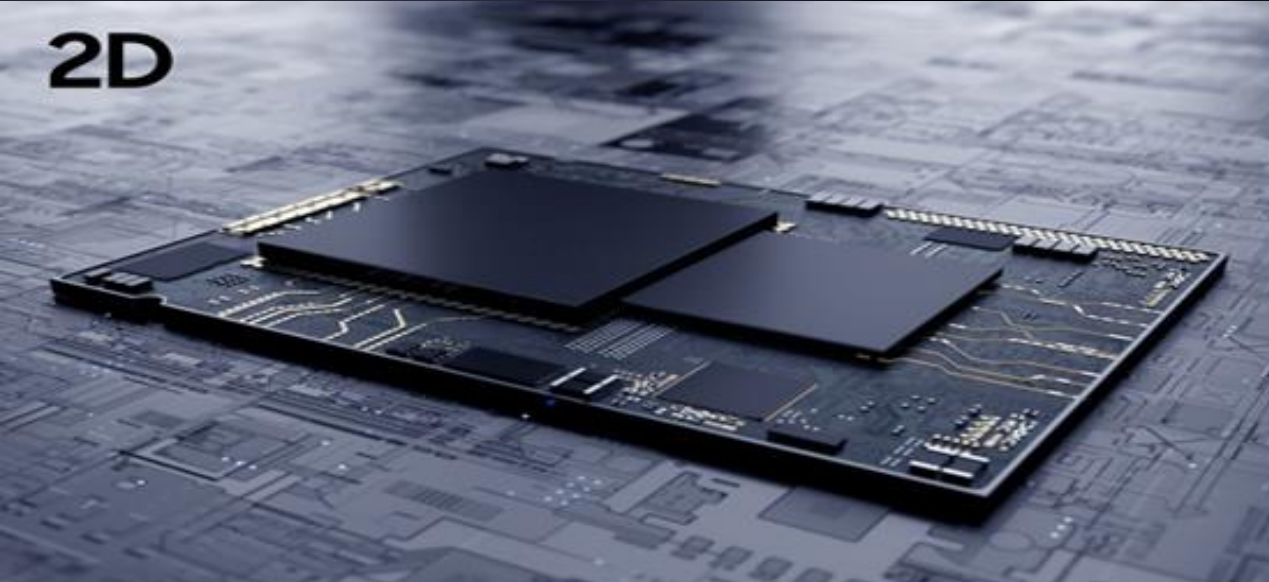


“Microprocessors – the most complicated devices ever made by man.”
Former Intel Corp. boss Craig Barrett

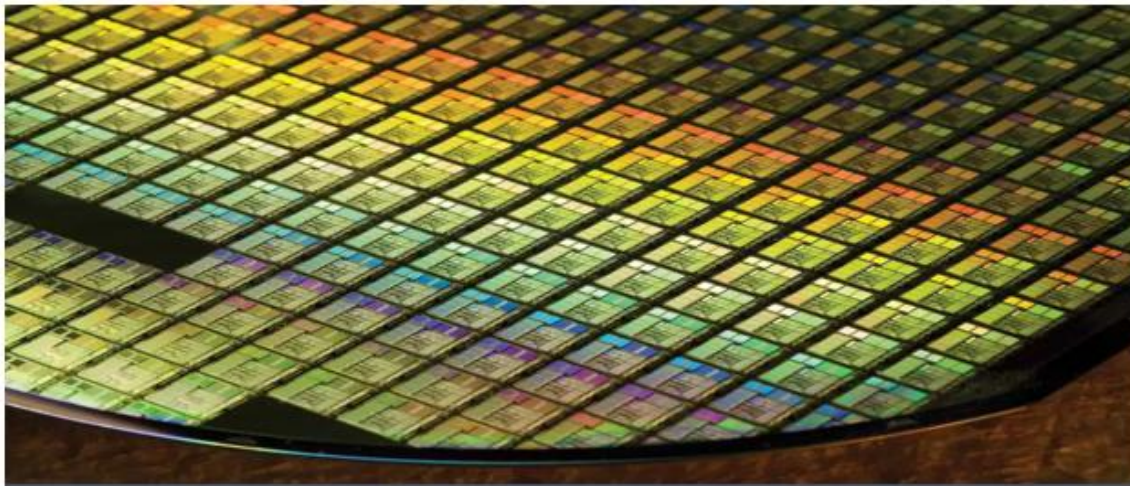




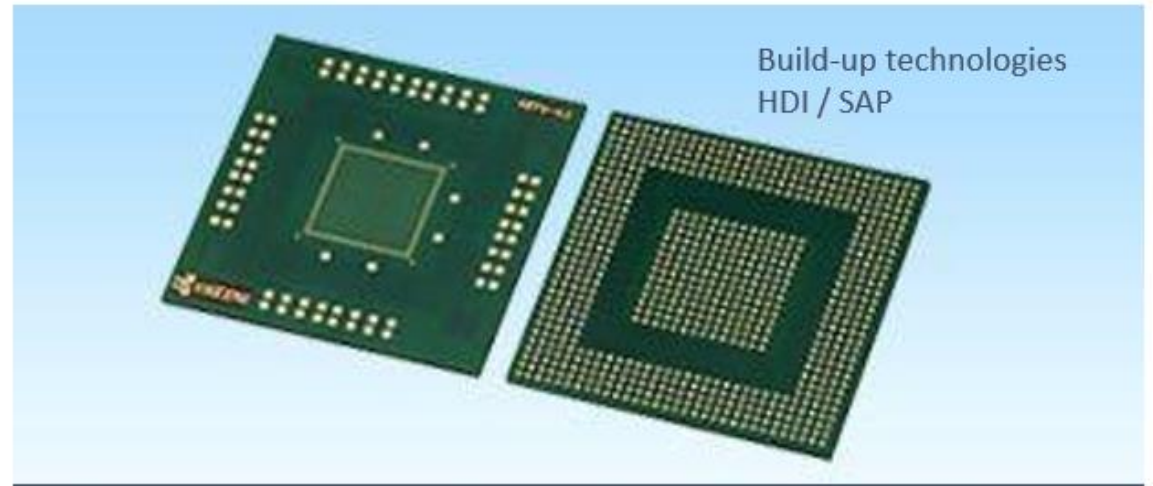
Samsung 2.5D I-Cube 4



Samsung X-Cube 3D TSV SRAM



1. Silicon Foundry & Fabrication – TSMC, Intel, Samsung



Build-up technologies
HDI / SAP

2. Organic Substrates – Ibiden, Shinko, Kyocera, TTM

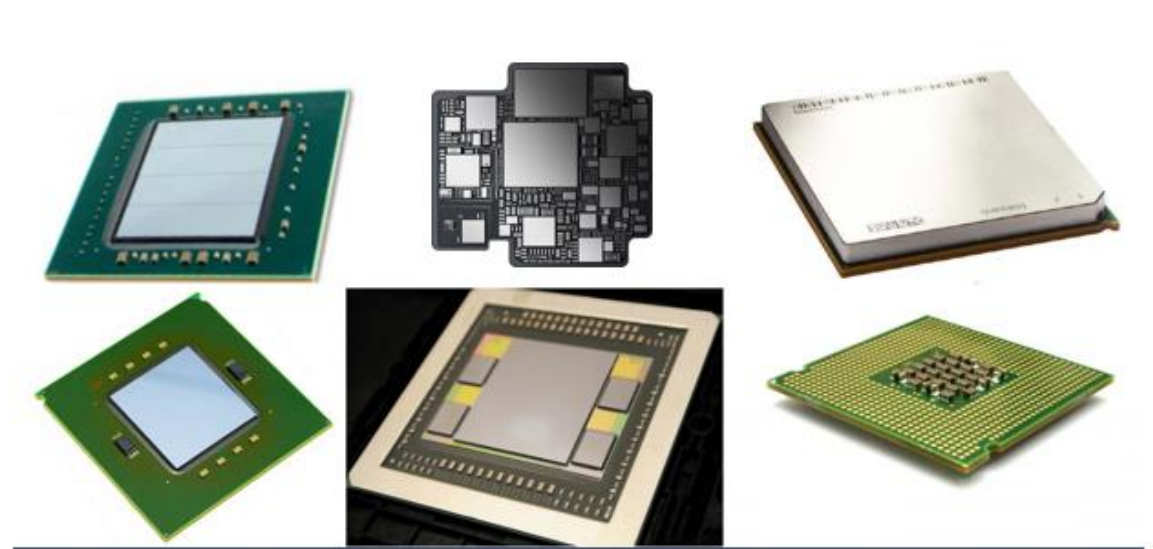
Model → Fabless
Own IP/Design
Partners Build



+ Custom Silicon
Google, Apple, Facebook, etc

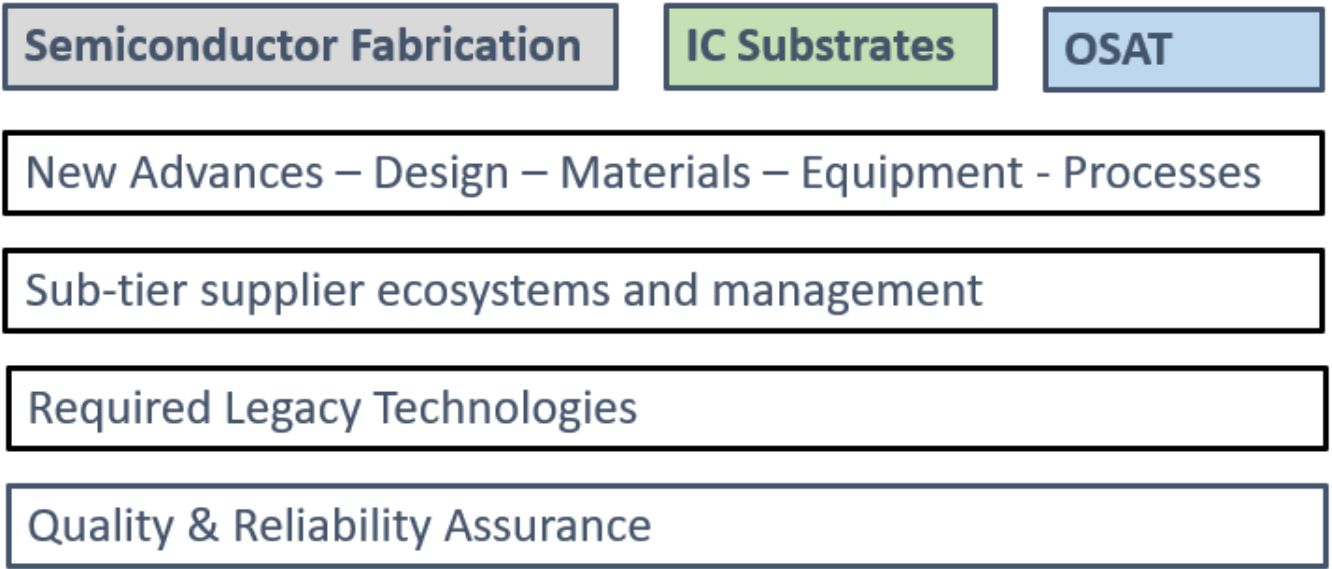
Many technologies
SCM, MCM, SIP,
PoP, 3D/2D, TSV

Advanced Packaging Logic Component Suppliers
Intel (x86), IBM, Xilinx, AMD, NEC, NVIDIA, TI, Broadcom



3. Semiconductor Packaging OSAT – Amkor, ASE, ChipMOS

End-to-End Semiconductor Advanced Packaging Ecosystem



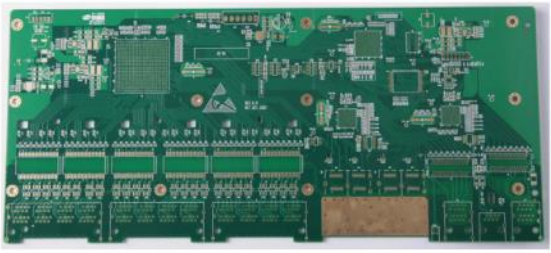
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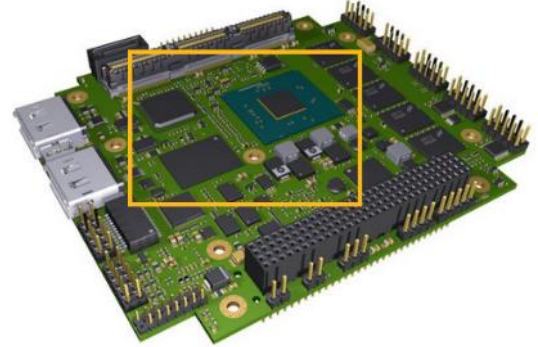
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Advanced Packaging Logic Component Suppliers
Intel (x86), IBM, Xilinx, AMD, NEC, NVIDIA, TI, Broadcom

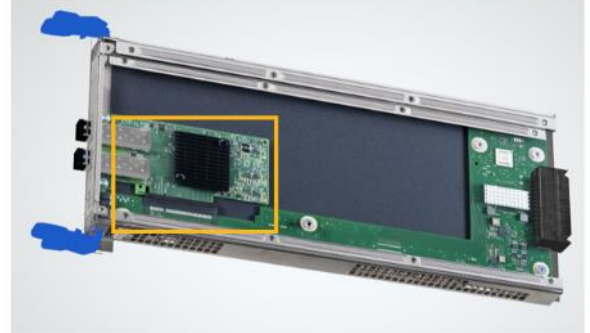
Electronic Components
Active / logic components (Processor, memory)
Passive discrete components (capacitors, resistors)
Connectors (power, USB, ethernet)



Printed Circuit Board (PCB)
Multi-layer plastic laminate w/ solder mask
Electrical connections - copper features and traces

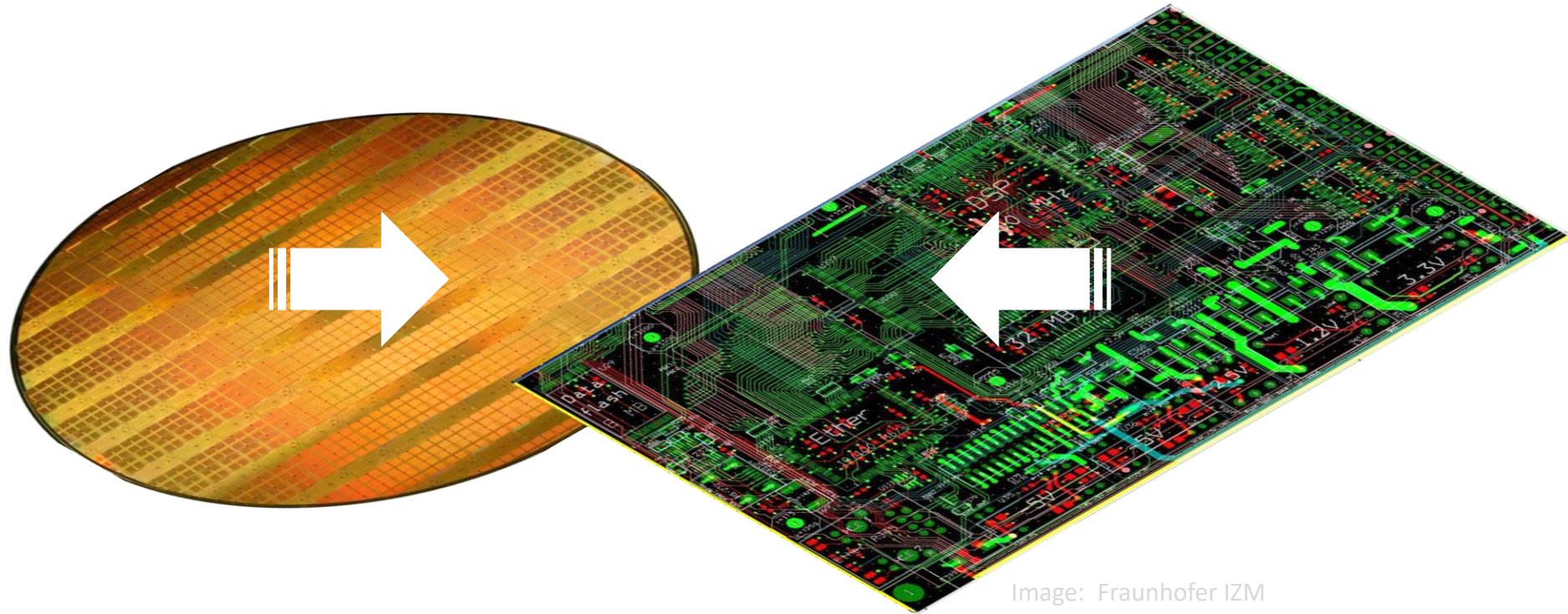


Printed Circuit Board Assembly (PCBA)
Printed Circuit Board (PCB)
Electronic Components
Interconnect joining materials (solder, adhesive)



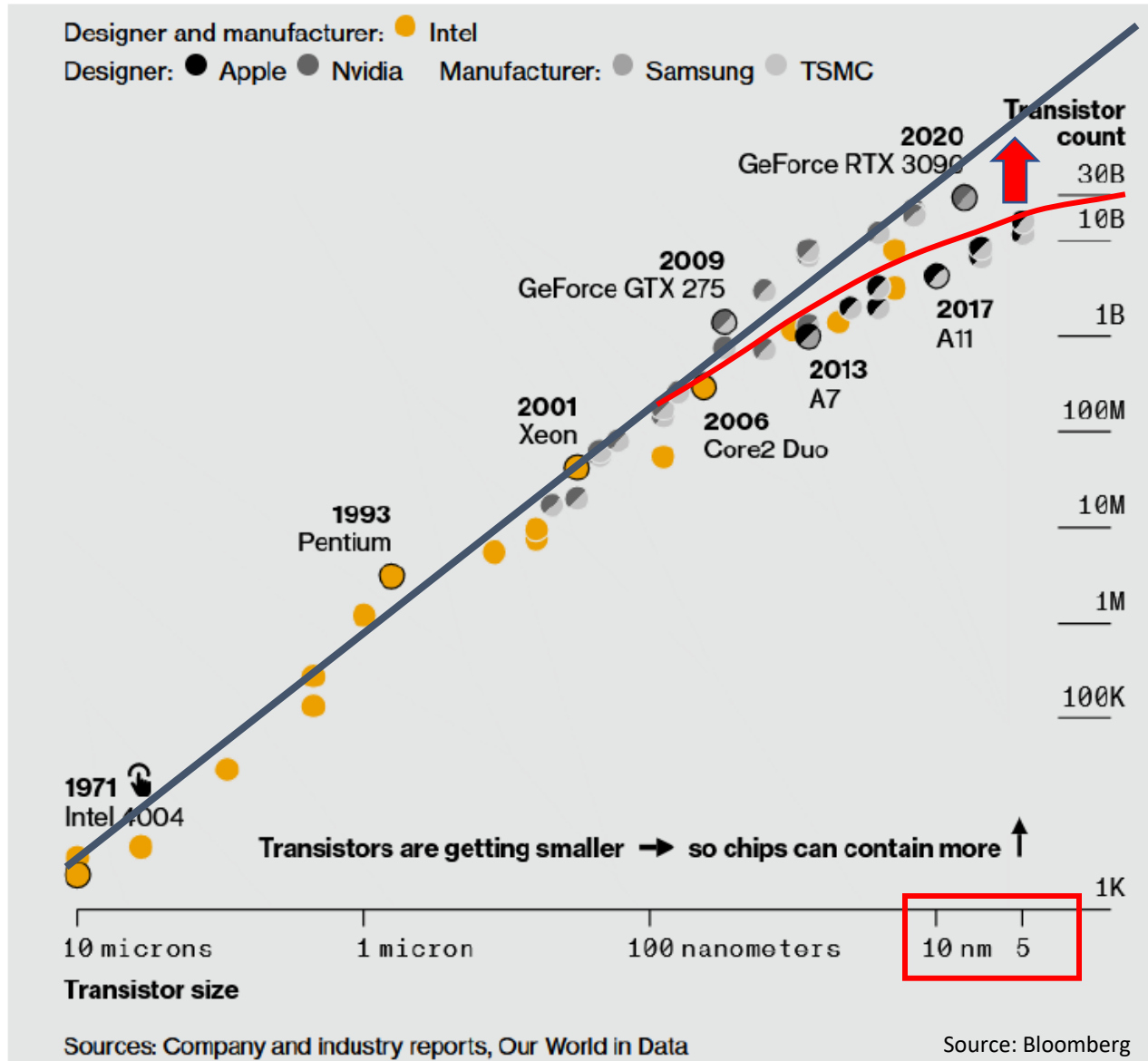
Printed Circuit Board Assembly w/ Mechanicals
Printed Circuit Board Assembly (PCBA)
Card-Level Mechanicals (heatsink, card bezel, screws)
Thermal Interface Materials

Future Trend: Gap Between Wafer Fab and System-Level Narrows



- **Advancing the state-of-the-art requires greater cooperation across the ecosystem**
→ IC design/fabrication, substrate, packaging, and system-level assembly

Moore's Law Challenges



Scaling - transistor size reductions continue
→ 2nm (2025), 1.4nm (2027), GAA transistors

Node reductions alone not sufficient anymore
→ **Chiplets and Heterogeneous Integration**

Silicon advances driving new packaging structures
→ **large variety of 3D packaging solutions coming**

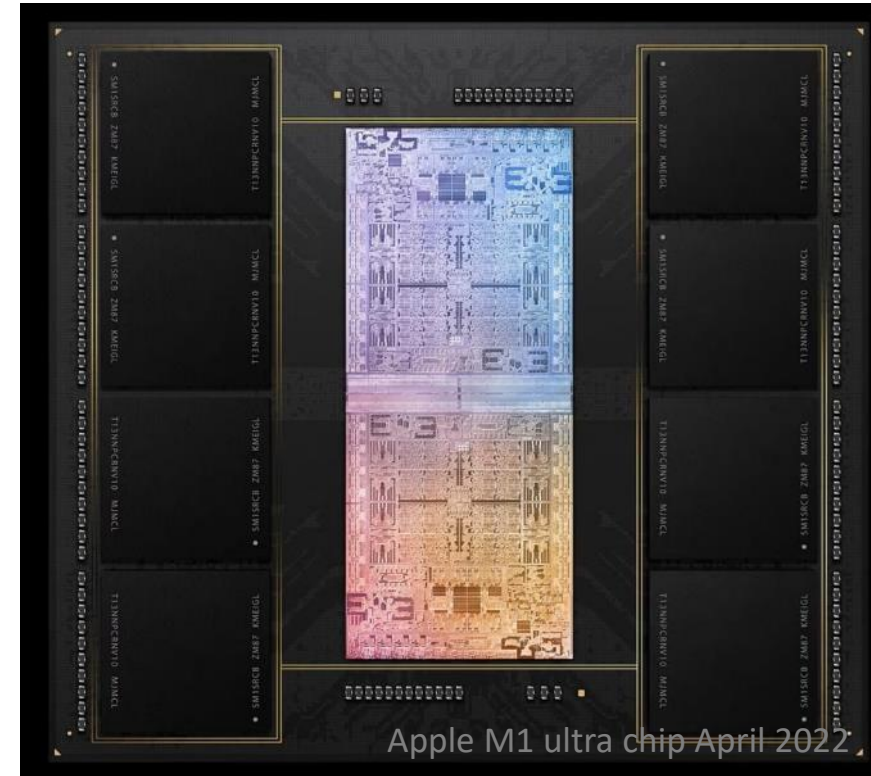
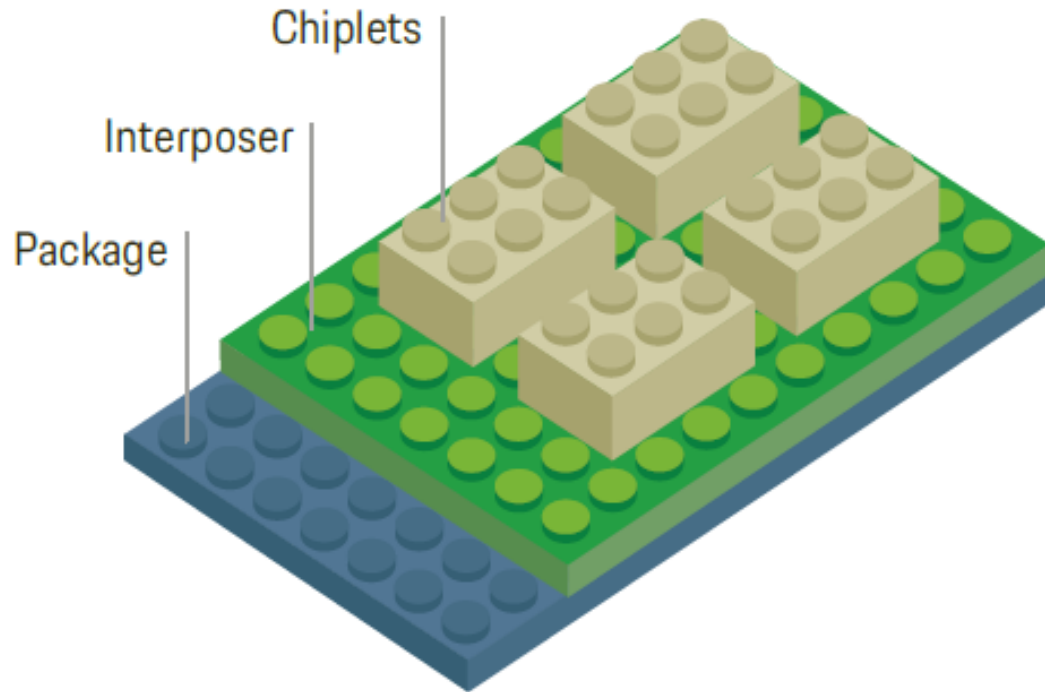
Research Focus

→ 3D packaging, materials thinning, energy efficiency

Semiconductor IP, design – North America, Europe
Substrates, packaging assembly, bumping – Asia

→ **Capability, capacity balancing needed**
North America and Europe

Chiplets, Heterogeneous Integration



- **Significant, Disruptive Change already in progress** – continue Moore's law trajectory
- Monolithic silicon → Chiplet architectures
- Miniaturization, functionality density, speed, performance
- Compute + memory + accelerators + storage → single package, many benefits

Global Semiconductor Supply Chain

North American semiconductor companies have migrated to the fabless model (Figure 1). The result is that the region is able to design next generation advanced packages but is heavily dependent upon Asian supply for chip manufacturing, IC-substrate production, and IC-packaging.

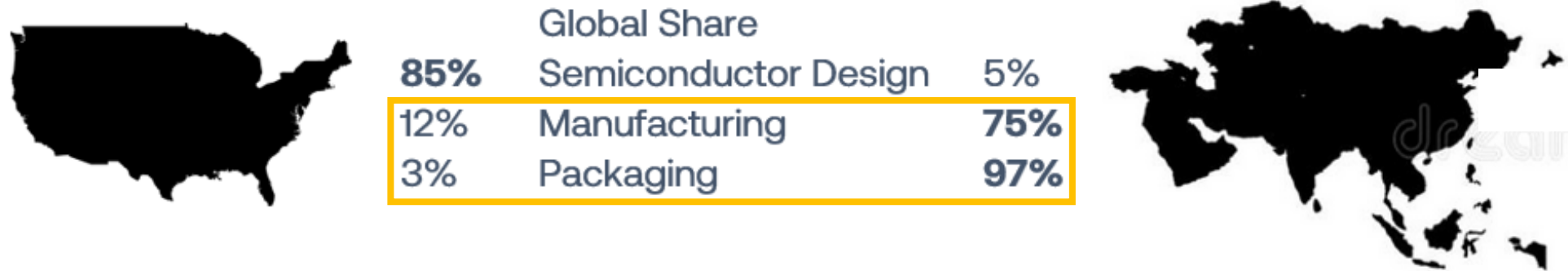


Figure 1: North American capability. Design focus, with outsourced manufacturing. Source: DoD Presentation

- Last 20 years – migration to low cost geos – labor, OpEx, margins
- Result today – unbalanced, many risks, NA and Europe lack fundamental capabilities
- **→ Need to rebalance: Regional + Global supply chain model**

> Study maps global ecosystems for advanced packaging, highlighting U.S. weaknesses amidst ongoing effort to spur domestic silicon fabrication.

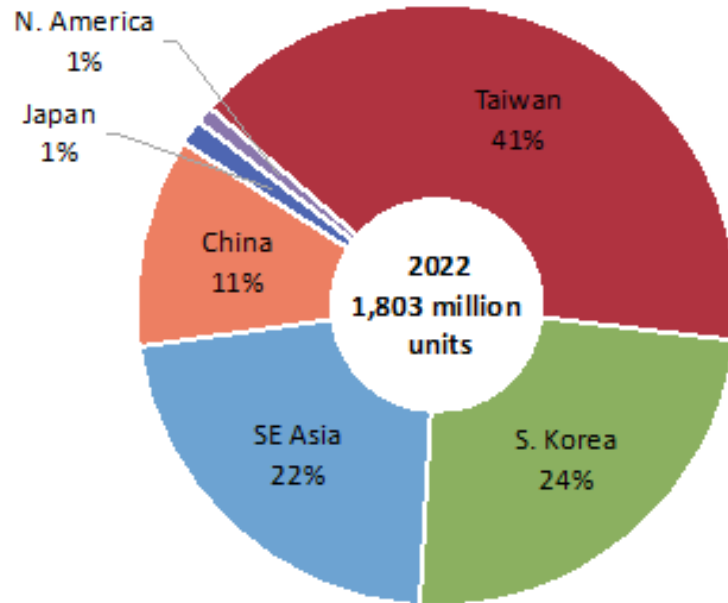


 Semiconductor Fabs  Semiconductor Foundries  IC Substrates  OSAT

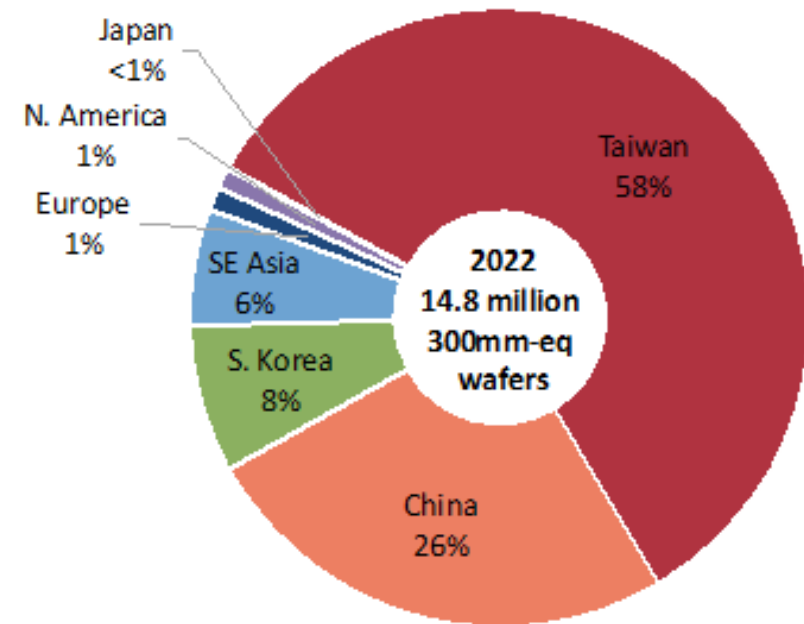
Global Advanced Packaging Capabilities

- Virtually no substrate or pkg assembly capability in North America or Europe

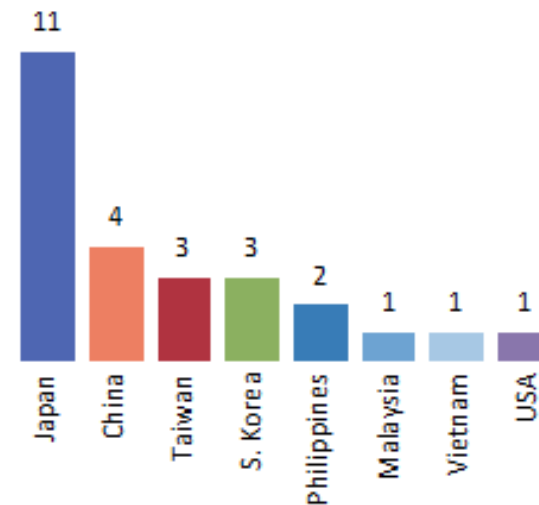
FC-BGA Assembly by Region



Merchant Bump Capacity by Region



Build-up Substrates Plants

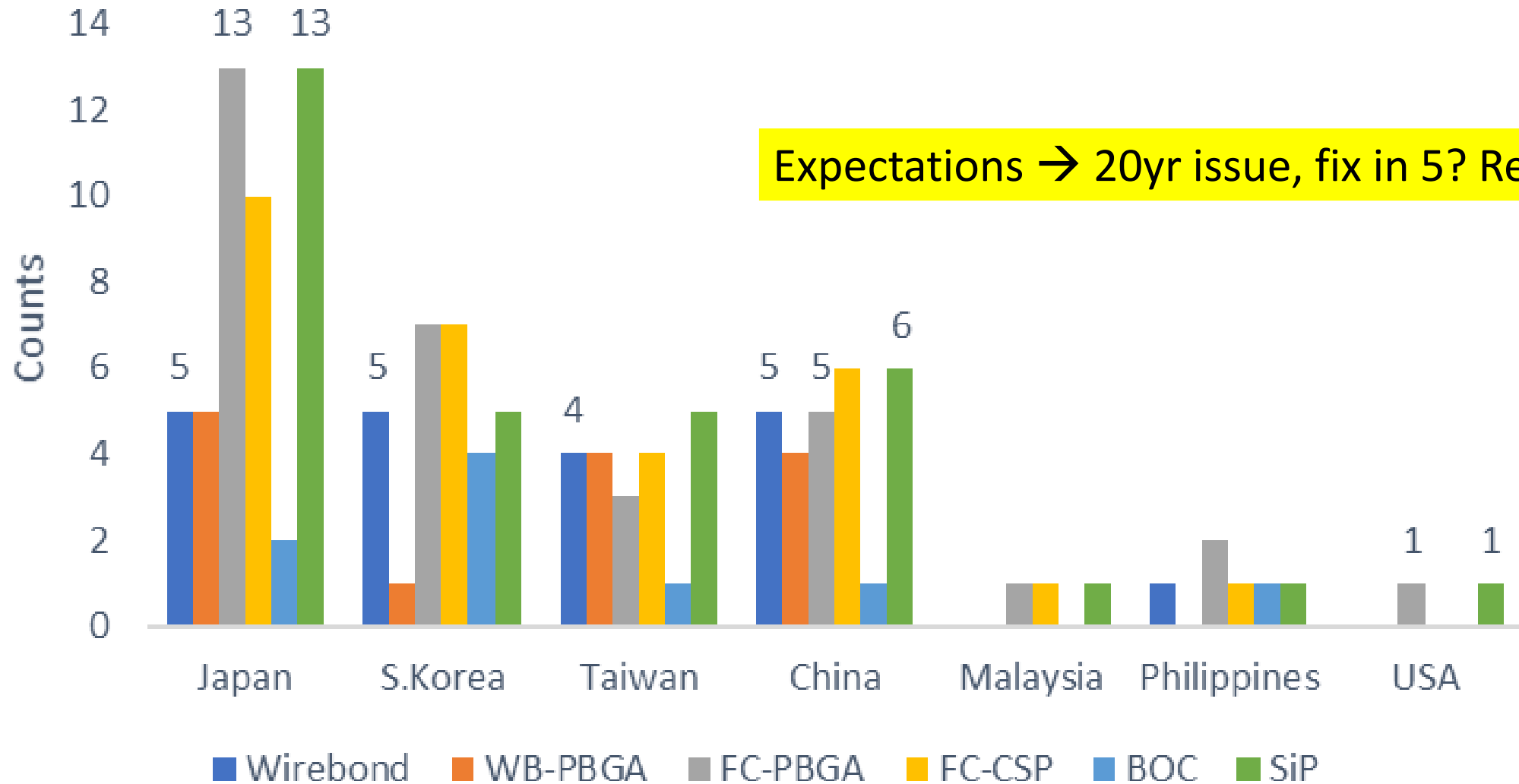


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U.S. Has Not Made Major Investments in Build-up Substrates

- > **Many years ago, U.S. PCB makers decided not to invest in IC package substrate production**
 - Endicott Interconnect had some capability in U.S. but unique material set (sold to TTM)
- > **Almost no capability in the U.S. to produce the most advanced IC substrates using build-up film to support high-density**
 - Substrate supplies concentrated in Japan, Taiwan, S. Korea, and a few in China
 - Some capacity in Philippines and Vietnam, planned for Malaysia
 - A few small suppliers located in U.S. but not with capability to support existing high-performance computing customers such as (Intel, AMD, Cisco, Broadcom, etc.)
- > **Advanced IC substrate requires state-of-the-art know-how, equipment, materials, and processes**
 - Most equipment and material suppliers located in Japan, rest of Asia, a little in Europe
- > **OK to use global supply chain, but...**
- > **Adding domestic semiconductor fab/foundries without a domestic IC-substrate supply and OSAT assembly will lengthen the supply chain, not shorten it**

IC Substrate Capability Counts by Region



Industry Response to Pending CHIPS Appropriations

US CHIPS Act

Microelectronics & Power electronics

RFPs expected May/June 2023

\$52B – majority semiconductor focused

EU CHIPS Act

Finalizing language/provisions

May/June expected release

■ Primary focus - microelectronics silicon (NSTC)

- > Minimal focus on microelectronics **substrates** or packaging assembly (NAPMP/MIIs)
- > **HDI, uHDI** PCB not a focus | advanced uPCBA not a focus

■ Minimal focus on power electronics

- > SiC, GaN WBG semiconductors main interest
- > **Low/mid-power organic substrates** or high-power ceramic substrates not a focus
- > 3D power packaging design and assembly development not a focus

■ Wider focus needed, not just silicon – enable final systems

- > Microelectronics & power critical elements – **Substrates**, packaging assembly, **uHDI PCB**, uPCBA

Many Different Packaging Options: All Use Build-up Substrates

> Silicon Interposers

- Xilinx (many FPGA products) started in 2012, AMD shipped in 2015 (GPU + HBM), NVIDIA (GPU + HBM), Google, Baidu, Broadcom, etc.

> Fan-Out on Substrate

- Chip first (in production since 2016 at ASE) and chip last solutions
- In production for network switch at TSMC with InFO-R (since 2018)
- Amkor Substrate-SWIFT®, SPIL Fan-Out Embedded Bridge, TFME

> Embedded bridge Intel, IBM, SPIL, TSMC, and others

- Intel's EMIB silicon bridge in an laminate substrate, embedded by substrate supplier (Intel Stratix 10 for AI accelerator)
- Amkor, ASE, IBM, JCET, SPIL, TSMC offerings

> RDL Interposers Samsung R-Cube™ and others

- Extend to finer feature (2 μ m L/S) switch to fab-like process

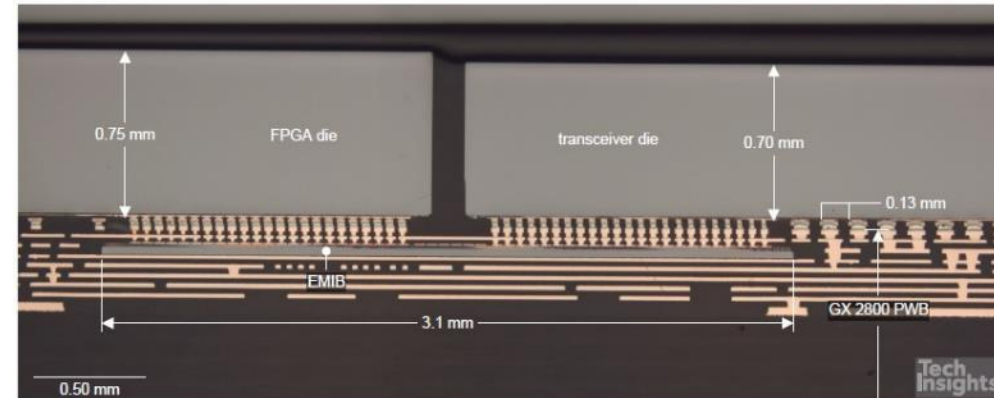
> 3D stacking

- AMD's 3D V-Cache™, Intel's Foveros, Samsung's X-Cube

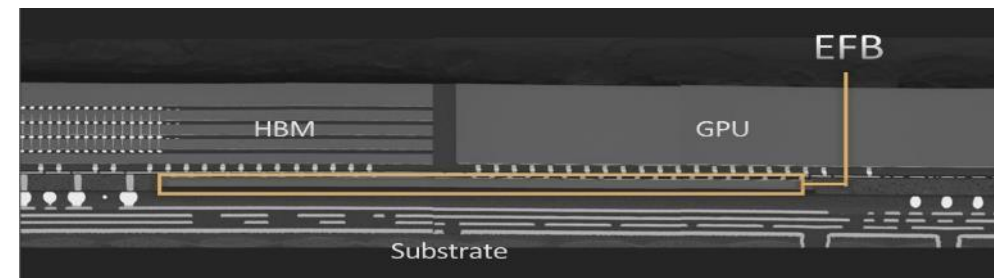
Source: TechSearch International Inc.



Source: NVIDIA



Source: TechInsights



Source: AMD

Microelectronic Substrates Roadmap

- No advanced substrate capability in US; Europe only in slightly better position
- R&D – L/S, layers, embedded elements, new build-up materials, alt cores
- **Chiplet architectures + advanced substrates** → unlocks new design capabilities

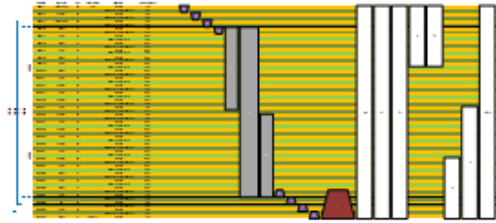
Attributes	Current tech State of the Art	Near term target (2-5Years)	> 5-10 years out (Grand Challenge)
Chip to Substrate/ Bump pitch (µm)	<100 (SOC)	<50 (chiplets/HBM)	<25? (chiplets/HBM)
Conductor line / space (µm)	9 / 12	5/5	2/2 or below 0.8um/0.8um (Stretched target)
RDL / build up via diameter (µm)	50	<25	<10
Body size (sq mm)	65x65	>100x100	>120x120
Layer counts	8 to 20	>20	>20
Ability to embed low density components	Si-Bridge, Capacitors	Capacitor, Inductor, IPDs	Integrated voltage regulators, encryption / security chips
Embedded Component Pitch (µm)	100	80	65

Source: ASIC

Substrate Materials for Advanced Packaging

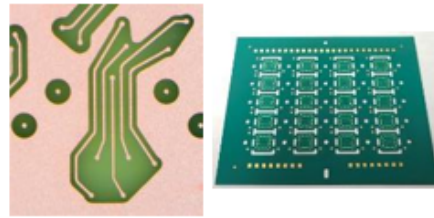
Options Include PWBs, Glass, and Silicon

High Density Interconnect



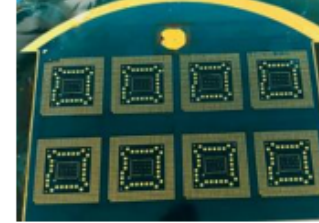
- High density PWBs with glass-weave dielectrics

High Density Build-Up



- Fine line/space organic laminate with Ajinomoto Build-Up Film

Glass



- Emerging glass-core tech with spin-on or laminate dielectrics

Silicon



- Interposer wafers with thru-silicon vias (TSVs) from Si fabs

Format	Panel	Panel	Wafer or Panel	Wafer
Min Line / Space	75 μm	< 12 μm	< 5 μm	< 2 μm
Min Pad Dia / Pitch	200 μm / 300 μm	<75 μm / <150 μm	~20 μm / 40 μm	<10 μm / <20 μm
Routing Layers	Many (30+ total)	7+ / side	4 / side	6+ / side
RF Performance	Good	Good	Moderate	Poor
Thermal Conductivity	Low	Low	Low	High
Thermal Expansion	High	High	Moderate	Low
Cost	Low	Low	Moderate \rightarrow Low	High

Sources: TTM, APCT

Source: Kyocera

Source: Georgia Tech

Source: Novati / Skorpis



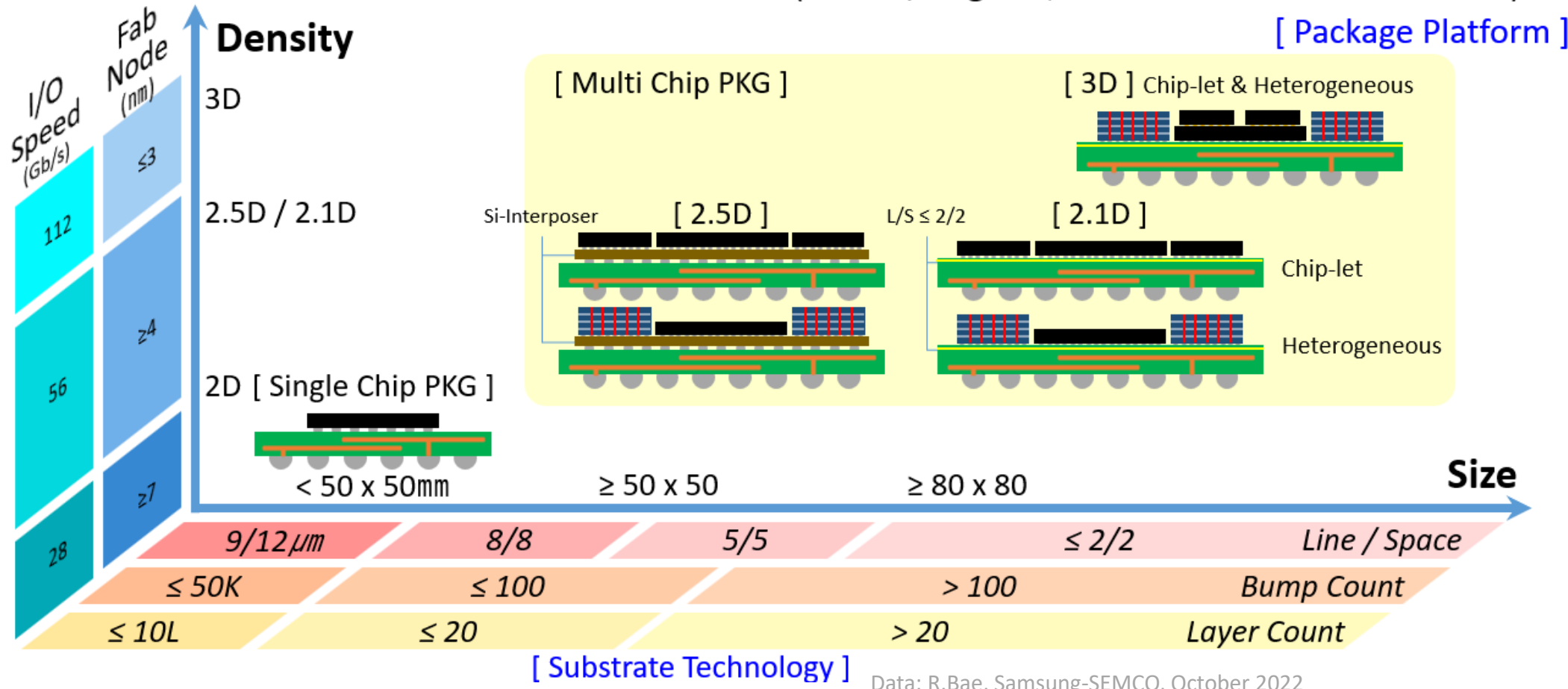
Substrate choice determined by performance, cost, and reliability for a given packaging case

Approved for Public Release; NG22-1778; ©2022 Northrop Grumman Systems Corporation

Data: H.Phillips, Northrop Grumman, October 2022
IPC Advanced Packaging Symposium, Washington, DC

Adopting Chip-let & Heterogeneous PKG Platform to Maximize Performance, Minimize cost

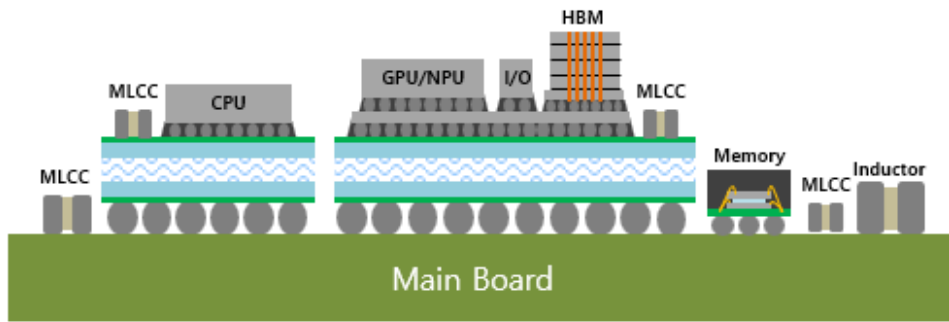
- Substrate Technology : Follows Foundry Technology Trend (Large Body, High Density, High Layer Count)
But base material is different (Silicon / Organic(※ Different Field of Technology including Machine))



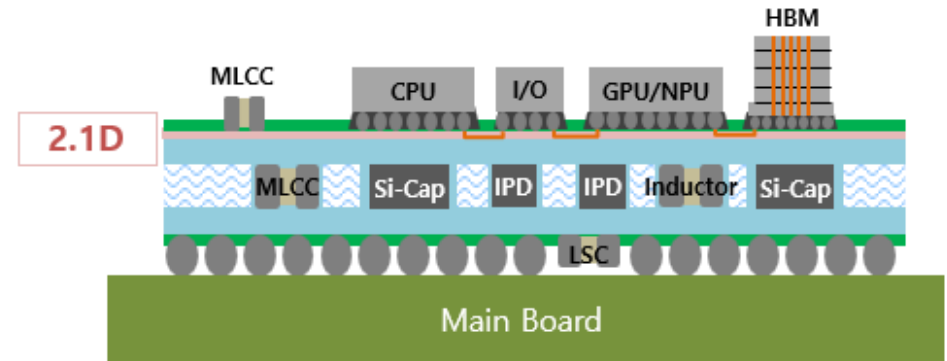
Data: R.Bae, Samsung-SEMCO, October 2022
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❖ SoS (System on Substrate) : New Platform to unify various systems on Substrate

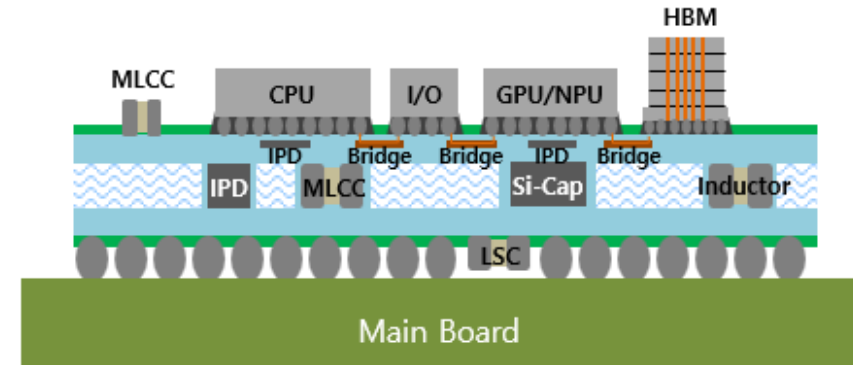
- Processor (CPU/GPU/NPU), I/O Chip, Memory, Passive, etc.



[Conventional]



[2.1D SoS Package]

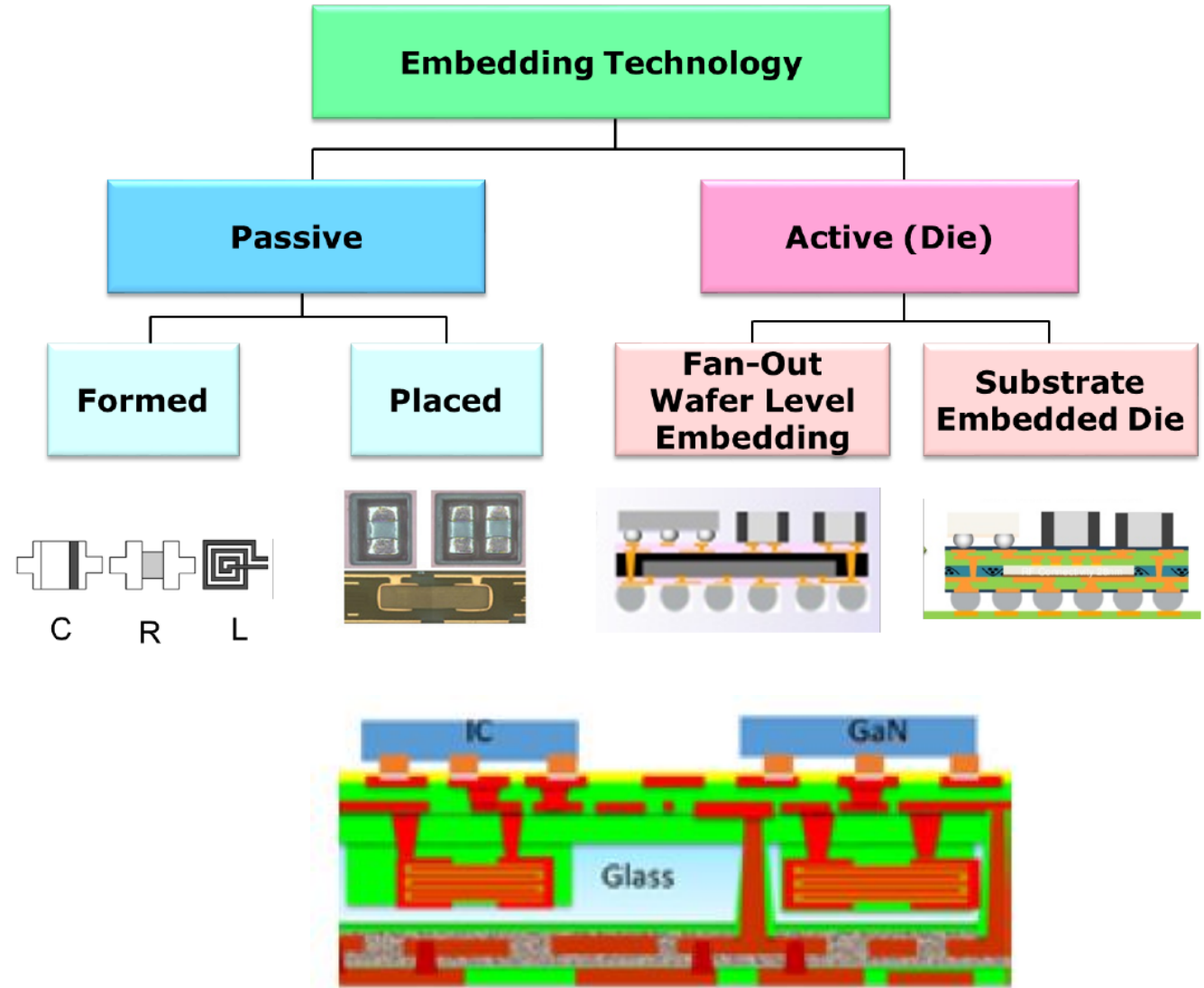


[Bridge SoS Package]

Data: R.Bae, Samsung-SEMCO, October 2022
IPC Advanced Packaging Symposium, Washington, DC

3D Power Packaging Similarities

- **HI/chiplets** → disruptive changes
- Common SiP approaches
- Performance, efficiency, density, cost
- **Advanced Packaging focus lacking** needs more attention/funding
- **Substrates** – similarities
 - > **Embedded actives/passives**
 - > Substrate build-up design, material, innovation, and reliability challenges
- NA / EU substrate capability and capacity needed
- **Speed of development limited by regional substrate capability/supply**



Source: PSMA 3D Power Packaging Phase III Report

Summary

- Period of significant disruption
- **Ecosystem approach needed** beyond semiconductors
- **'Advanced packaging is the new king'** beyond silicon scaling
- Need to rebalance → Regional + Global supply chain model
- Catch-up vs. leapfrog
- Future speed of innovation enabled by full ecosystem
- **Significant need for improved substrate capability & capacity in NA and EU**
- **Many similarities b/t microelectronic and 3D power substrates – embedded technologies**

- **IPC Advanced Packaging Leadership Council (APL)**
 - > **Scope: Microelectronics + Power Electronics**
 - Substrates, uHDI, uPCBA
 - Narrowing gap – 1st level packaging and system-level assembly

Call to Action

While North America and Europe are talking, Asia is doing – gap is getting bigger every quarter

- If chips only focus, then extending the supply chain not shortening it
- Substrates and Packaging Assembly are critical. Not just Silicon.

US lacks build-up substrate capability, adv pkg assembly capacity – Manufacturing Matters

- Near term – business issues to enable state-of-the-practice (capacity)
- Longer term – overcome technology issues, R&D

Change mindset – fail fast, iterate, learn, increased rate and pace needed

Thank you. Questions?

We must *all be advancing* – ‘**Silicon to Systems**’ approach

If we are going to build sustainable, regional/global advanced packaging and system assembly ecosystems – we need Governments, Commercial Industry, Academia to continue collaborating, developing, executing.

Collaborate – Modernize – Transform

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