Vertical Integrated High Density Power Packaging Technology

CP Hung, Mark Li and Vikas Gupta

ASE Group

vikas.gupta@aseus.com

ASE Confidential / Security-B

Outline

- **Technology Overview**
- **Power SiP Technologies**
  - aEASI
  - SESUB
  - Double Side SiP
  - 3D Power SiP
- **Integrated Power in u-Processor**
  - Advanced Packaging
  - Inductors
  - Capacitors
- **Summary**

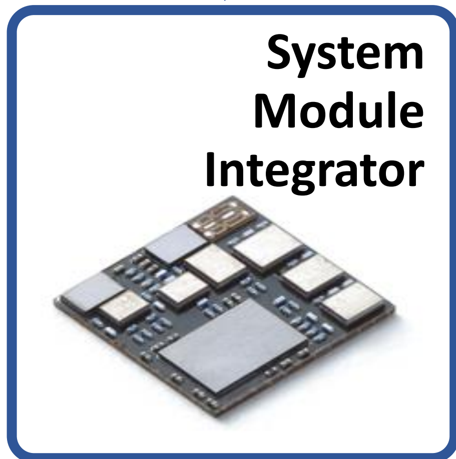
© ASE Group. All rights reserved.

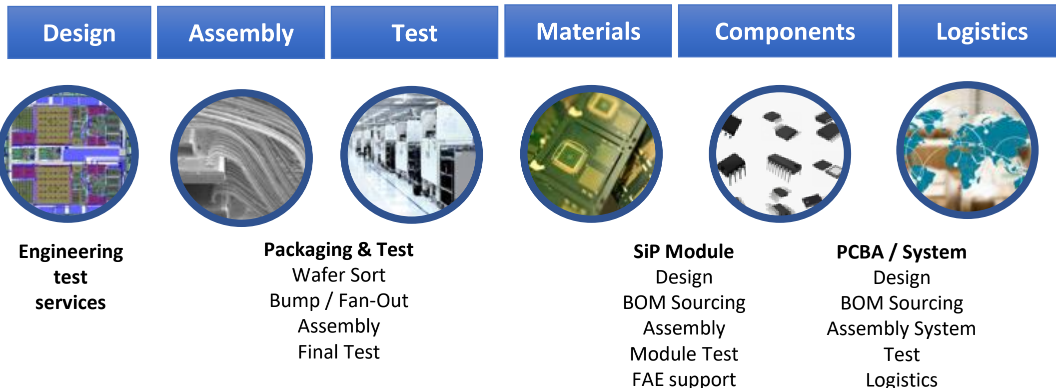
Application Integrated Solution

OSAT

Application-Specific

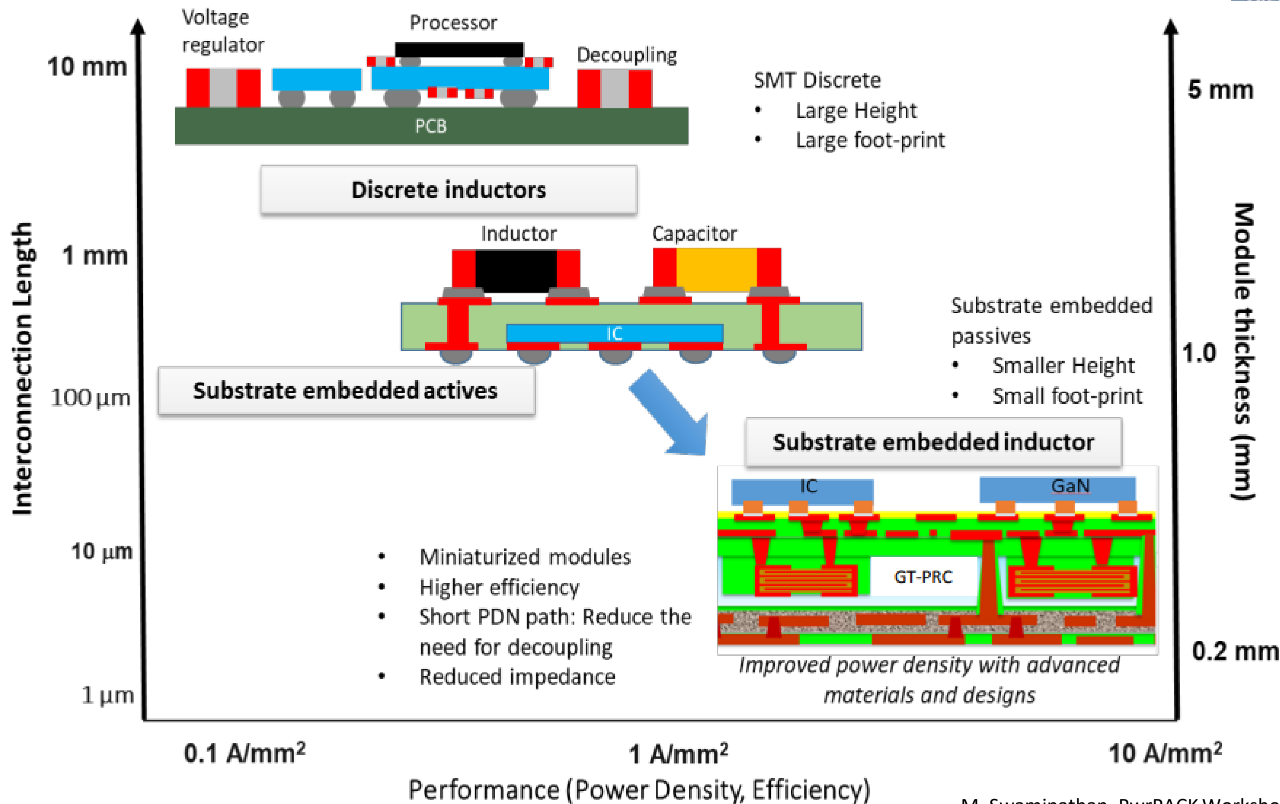
EMS





© ASE Group. All rights reserved.

Power Delivery Trend



M. Swaminathan, PwrPACK Workshop 2019

Focus of this presentation

1. **Packaging technologies for miniaturization from board level to sub modules levels; higher efficiency and reduced impedance**
2. **Integrated power solutions encompassing 2.5/3D package configurations and high-performance passives**

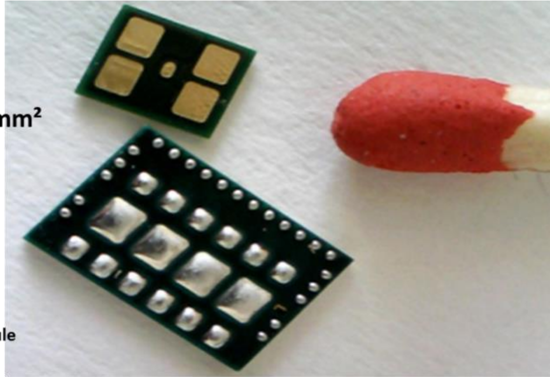
© ASE Group. All rights reserved.

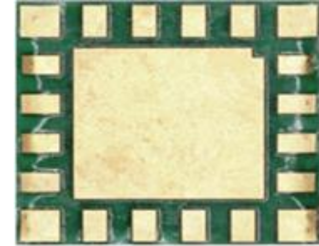
Outline

- Technology Overview
- **Power SiP Technologies**
  - aEASI
  - SESUB
  - Double Side SiP
  - 3D Power SiP
- Integrated Power in u-Processor
  - Advanced Packaging
  - Inductors
  - Capacitors
- Summary

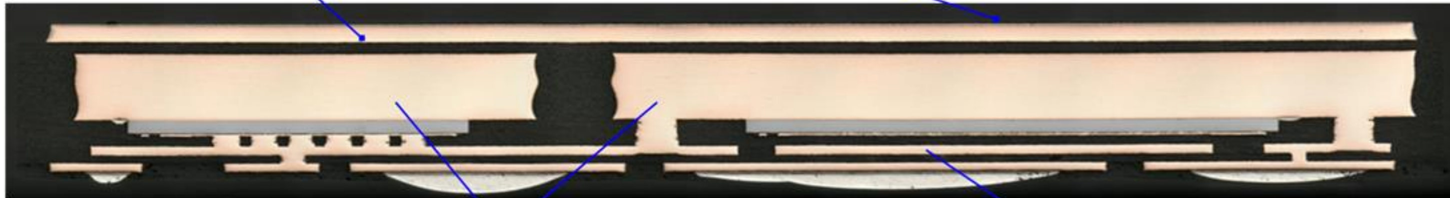
© ASE Group. All rights reserved.

aEASI (advanced Embedded Active System Integration)



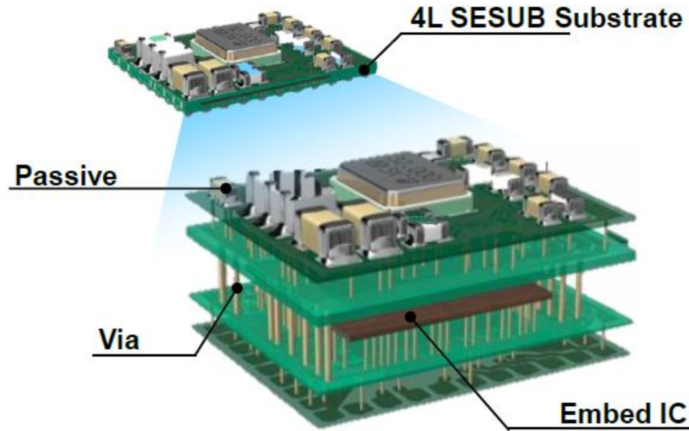


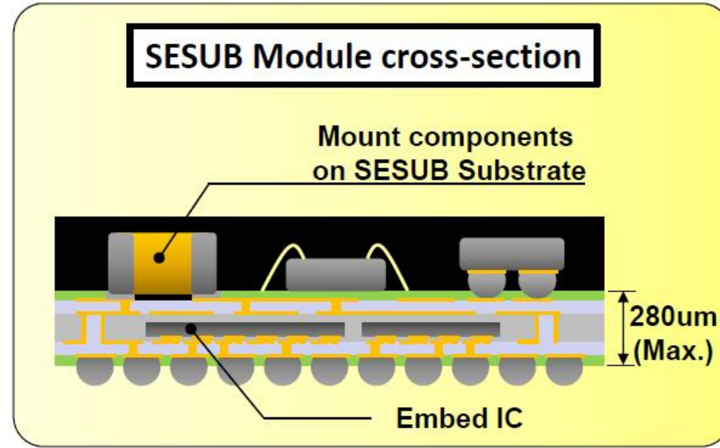
aEASI Size: 5 x 5 x 0.57 mm^3 (exclude passives height)
1 Micro Power Chip with RDL: 2+1 Layer
Passives: 12 (0806 x 2, 0603 x 2, 0402 x 4, 0201 x 4)
>100KK units shipped



© ASE Group. All rights reserved.

SESUB (Semiconductor Embedded in SUBstrate)





- IC wafer grinded to 50um and embedding in resin substrate
- Total substrate thickness 280um or below
- Multiple dies could be embedded in a SESUB

© ASE Group. All rights reserved.

SESUB Construction (4 Layer)

Single Die embedded for 4 Layer Structure

Core

Solder Resist

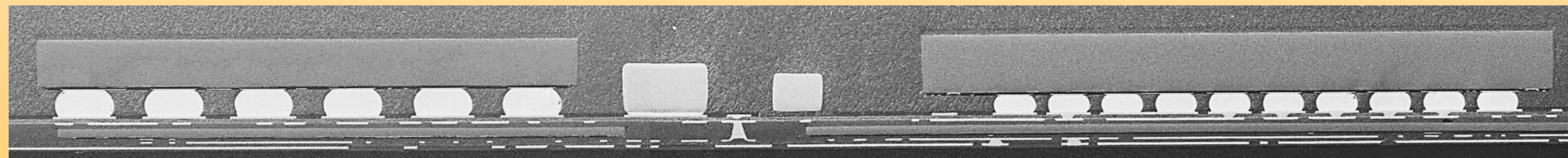
RDL on Die

Outer Layer Blind Via

Via on RDL of Die

Inner Layer Blind Via

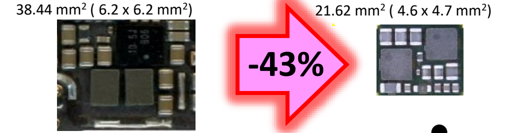
Two dies embedded in 4 Layer SESUB (2 WLPs and Passives on SESUB)



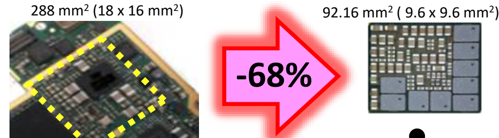
© ASE Group. All rights reserved.

Embedded for Size Advantages

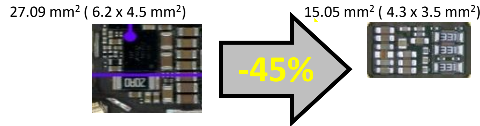
- Camera Power Module



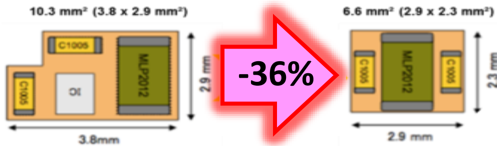
- Power Management Unit Module



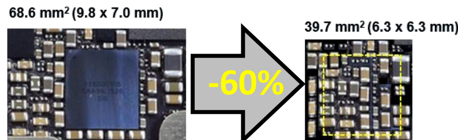
- Wireless Charge Rx



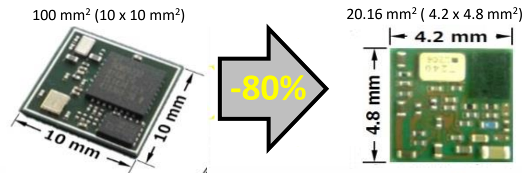
- μ DC-DC Convertor Module



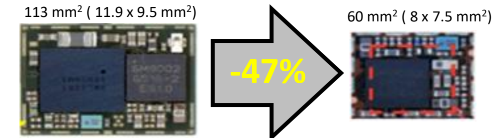
- Audio Module



- Bluetooth Low Energy Module



- WLAN Module

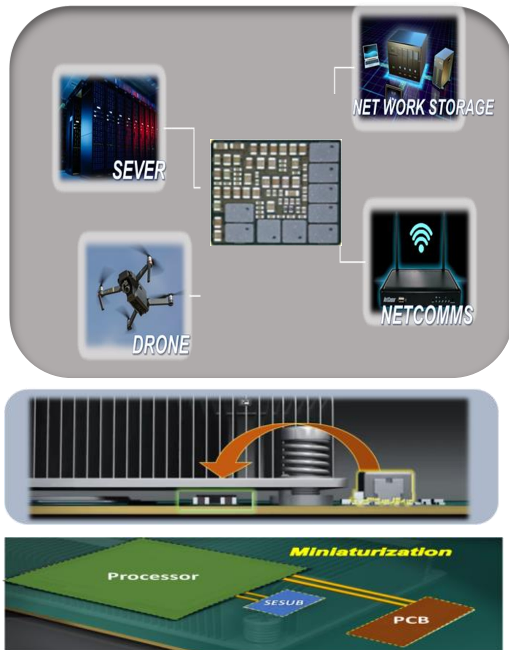


© ASE Group. All rights reserved.

SESUB Applications and Production Summary

>50KK units shipped for each of the applications

PMIC



- X/Y/Z dimension reduction
- Shorter transmission path
- In HVM

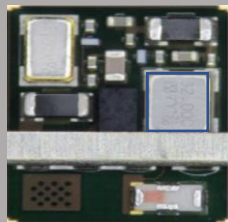
Consumer Application

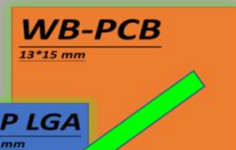
- Camera Power Module

38.44 mm² (6.2 x 6.2 mm²)

21.62 mm² (4.6 x 4.7 mm²)

Area -43%



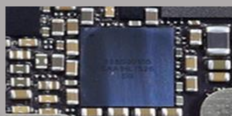


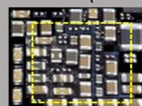
- Audio Module

68.6 mm² (9.8 x 7.0 mm)

39.7 mm² (6.3 x 6.3 mm)

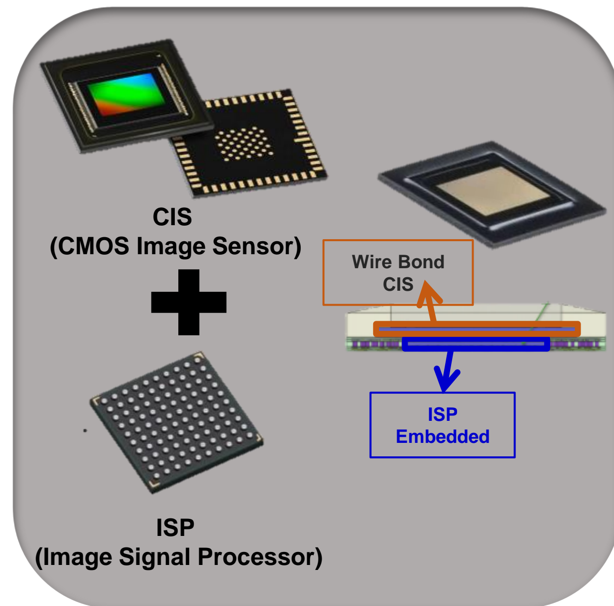
Area ~60%





- Miniaturization
- In HVM

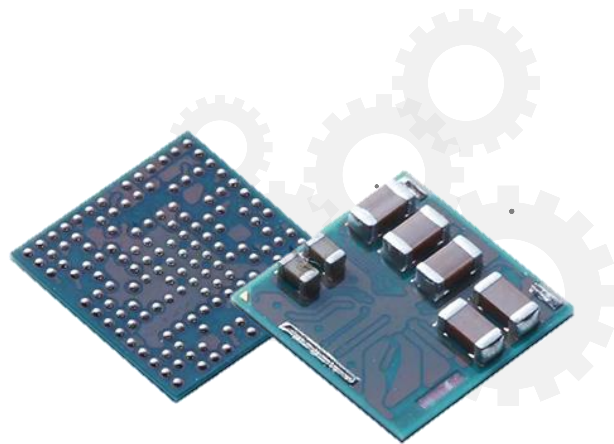
Automotive



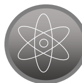
- Excellent signal performance
- Better thermal dissipation
- In HVM

© ASE Group. All rights reserved.

SESUB Reliability Experience

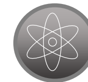


Reliability



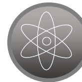
Precondition

TCT -65℃~150℃*5x
Baking 125℃*24hr
(MSL3)30℃/60% RH *192hr
Reflow 260℃*3x



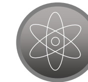
PCT

Temp:121±2℃ , ,100% RH,
Vapor pressure: 29.7Psia, Time: 96hr



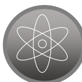
uHAST

Temp:130℃ , RH : 85%
Pressure: 33.3Psia, 96 hours



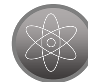
Solderability

PC: Steam Aging B, Flux angle: 45 ,Fluxtime:5~10s,
Temp:245±5℃,5±0.5s,
Rate: 25±6mm/s



HTST

Temp: 150℃ ,Time: 1000 hours

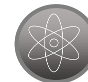


LTST

Temp: -40℃,Time: 1000 hours

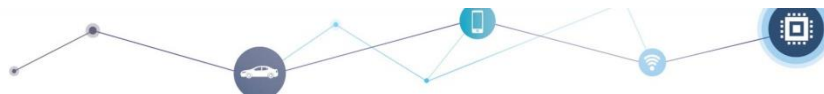
TCT

Temp:-55℃~125℃
mode: 1000/2000 cycles



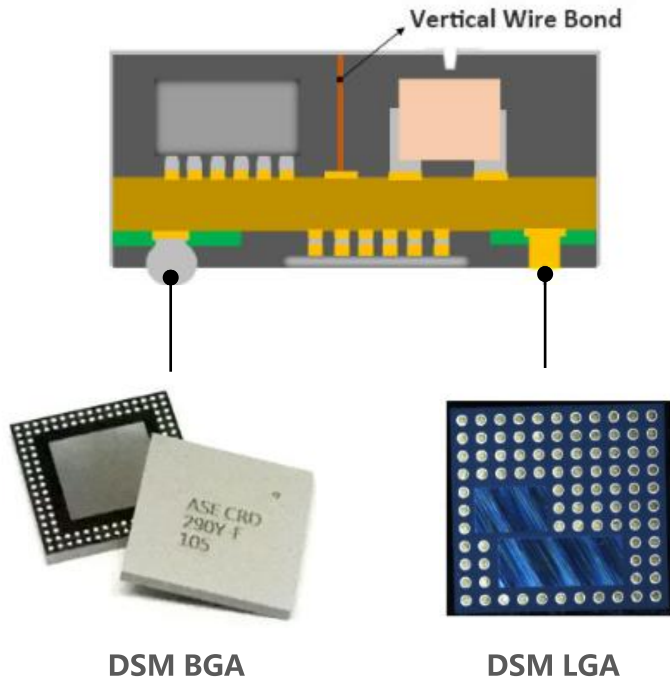
Multi Reflow

Temp: 260℃ , 30 cycles



© ASE Group. All rights reserved.

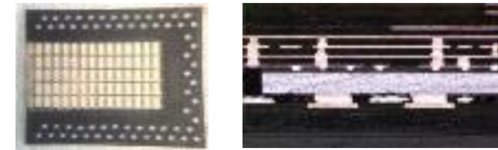
Double Side SiP



DSM BGA

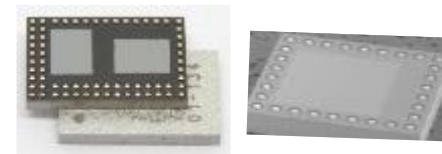
DSM LGA

- Double side reduced 20~40% area
- DSM Low Profile < 0.8mm



8.6x9.6x1.01mm
Thermal pad for high power design

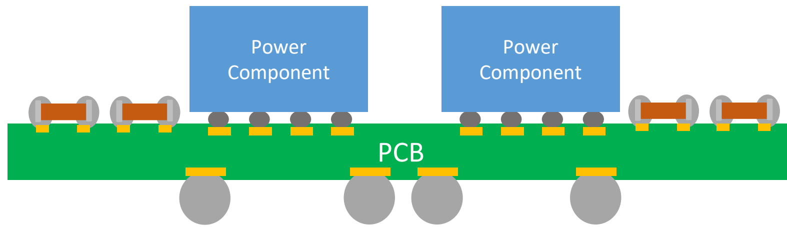
3.8x5.6x0.8mm
Laser ablation around ball

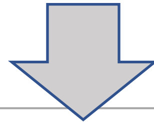


3.7x4.2x0.7mm
Grinding for thinning

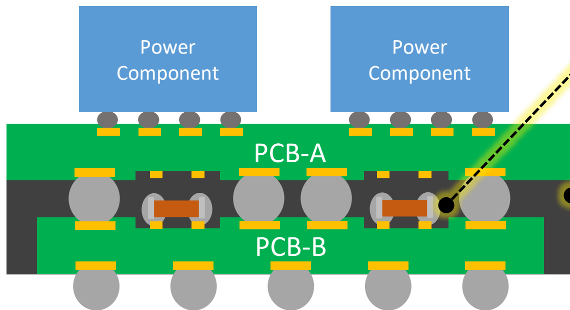
© ASE Group. All rights reserved.

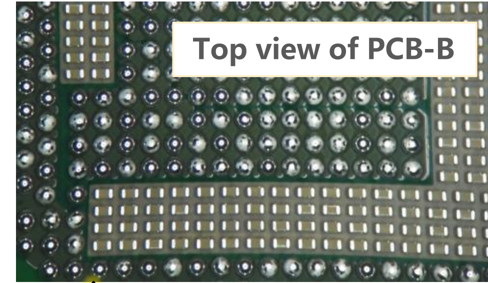
3D Power SiP

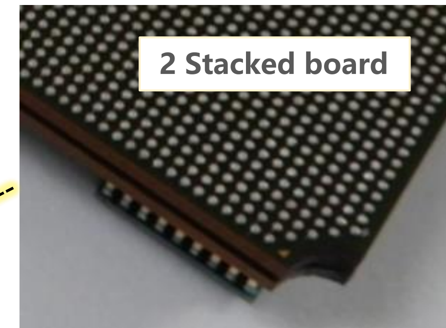




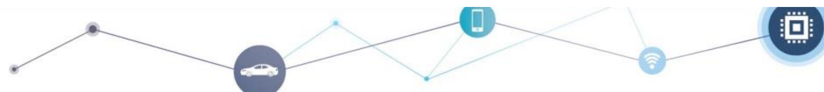
Integrate Capacitors (>500ea) on PCB_B;
Assemble PCB_B on PCB_A





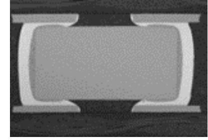


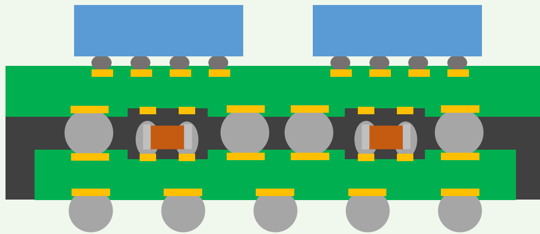
- Enhance PDN performance
- Compact Size
- Mass production in 2023



© ASE Group. All rights reserved.

3D Power SiP Roadmap



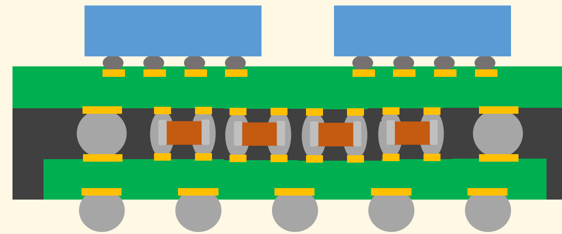


3D Power SiP 1.0

- Connect Capacitors to Bottom PCB
- Enhance PDN performance
- Integrate capacitors (~500ea)

In Qualification

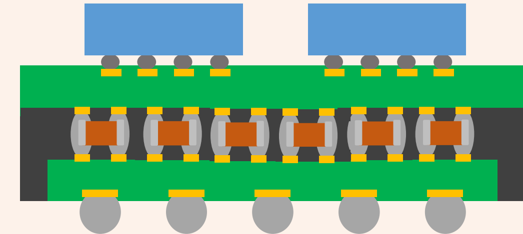
Production 2023



3D Power SiP 2.0

- Connect Capacitors to Top & Bottom PCB
- Further enhance PDN performance
- Integrate more capacitors (~1000ea)

In Development



3D Power SiP 3.0

- No solder ball between Top & Bottom PCB
- Better joint quality
- Integrate more capacitors (~1500ea)

© ASE Group. All rights reserved.

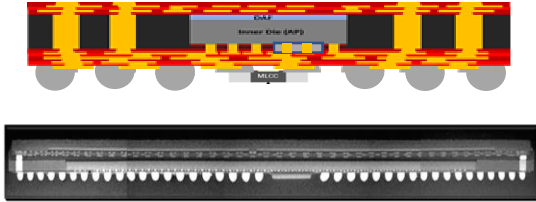
Outline

- **Technology Overview**
- **Power SiP Technologies**
  - aEASI
  - SESUB
  - Double Side SiP
  - 3D Power SiP
- **Integrated Power in u-Processor**
  - Advanced Packaging
  - Inductors
  - Capacitors
- **Summary**

© ASE Group. All rights reserved.

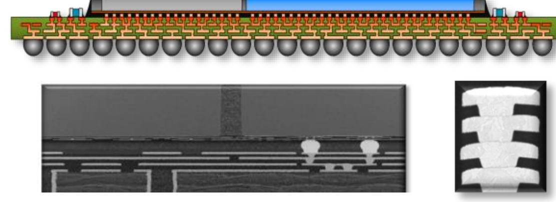
VIPack™ Platform – RDL Based Vertical Integration

VIPack™ Pillar I: FOPoP



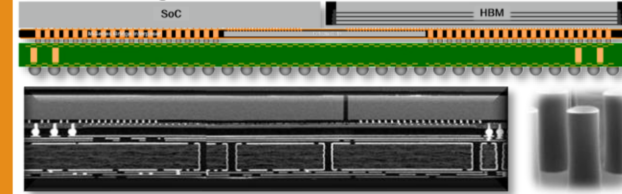
- ❑ Lowest Profile POP Package <330um
- ❑ Multiple RDL Routing Planes
- ❑ Balanced Construction
- ❑ Multi Die Capable for HI, DTC Integration

VIPack™ Pillar II: FOCoS



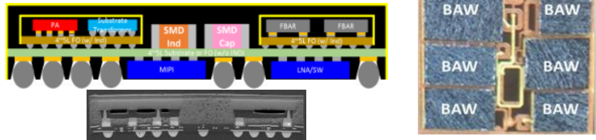
- ❑ High Density Fan-Out Single or Multi Die
- ❑ Chip First or Chip Last Integration
- ❑ 1.5/1.5um Line/Space, 6 metal layers, 32x38FO
- ❑ Flip Chip attached to RDL or Organic Substrate
- ❑ HBM Integration via RDL-Non-Bridge Die

VIPack™ Pillar III: FOCoS - Bridge (Embedded)



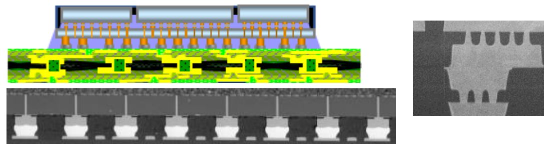
- ❑ Multi Die Attached to Both Sides of an RDL stack
- ❑ Bridge Die, DTC, VCO, etc. Integration
- ❑ Advanced HBM Integration & ASIC Disaggregation
- ❑ M-Series Integration Options

VIPack™ Pillar IV: FOSiP for RF Module



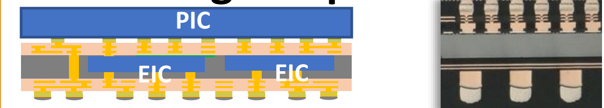
- ❑ Lowest Profile DS-SIP
- ❑ Multi- Pkg Integration
- ❑ Ultra High -Density Component Spacing
- ❑ Multi Layer RDL Stack w/Stacked Vias & integrated passives

VIPack™ Pillar V: 2.5D/3D IC



- ❑ Sticked interposer for large die area->1.6 reticle
- ❑ L/S <1um up to 5 layers
- ❑ 3D- TSV Last, MEOL, Hybrid Bond
- ❑ Integrated Passives in RDL

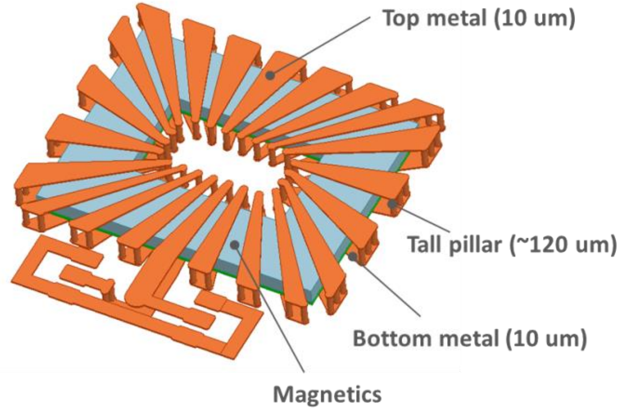
VIPack™ Pillar VI: Co-Packaged Optics

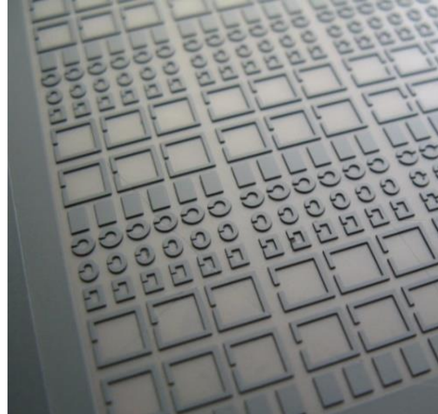


- ❑ Extends roadmap of SERDES HS Interface
- ❑ High Integration of PIC/EIC Die- Perf
- ❑ V-Groove Alignment DRIE
- ❑ Option- Embedded RDL for Die Integration

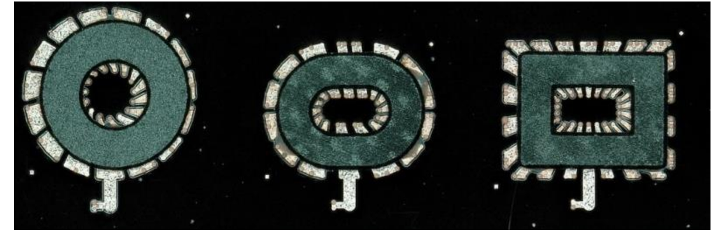
© ASE Group. All rights reserved.

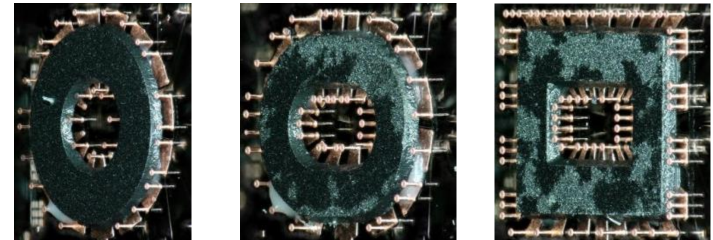
3D Tall Pillar Inductor





Magnetics from 3rd party

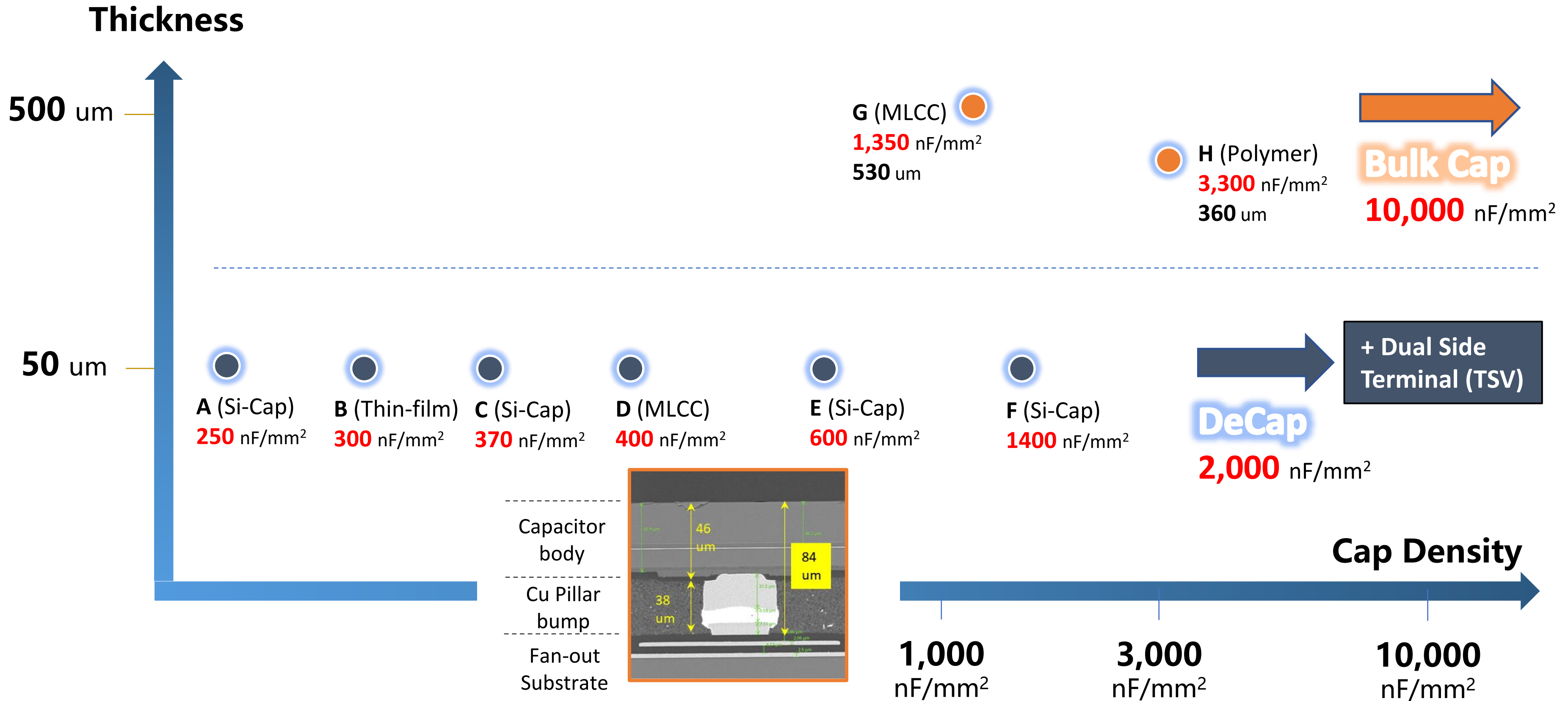




Top view and 3D view

© ASE Group. All rights reserved.

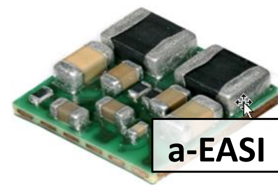
Capacitor Benchmark & Options

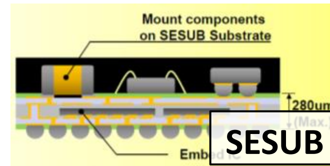


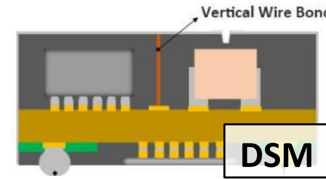
© ASE Group. All rights reserved.

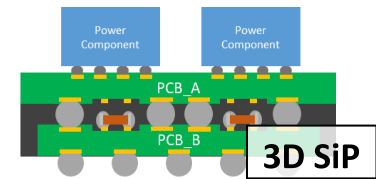
Summary

- **High power density for wide array of applications through Vertical Power Integration using ASE SiP Technology**

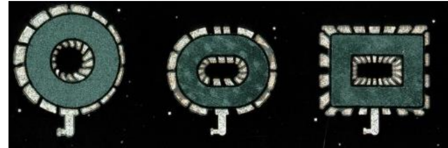


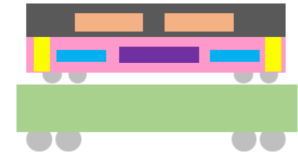




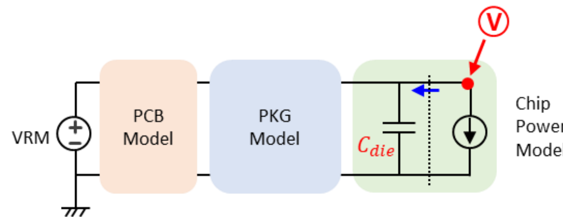


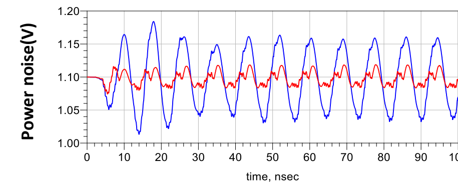
- **Enabling 2.5D 3D package platforms (and associated PDK's) with integrated VR, Inductors, and Capacitors in collaboration with designers, passive component/ magnetic suppliers**

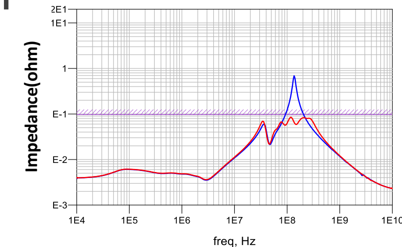




- **Coupled with co-design expertise to optimize package design including power integrity analysis, ball map and decoupling capacitor allocation**







© ASE Group. All rights reserved.

Thank You

Acknowledgements:
Kay Essig, William Chen and Mark Gerber

ASE GROUP
日月光集團

www.aseglobal.com