NMOS/NLDMOS LSS dead-Time Minority Carrier Isolation Optimization

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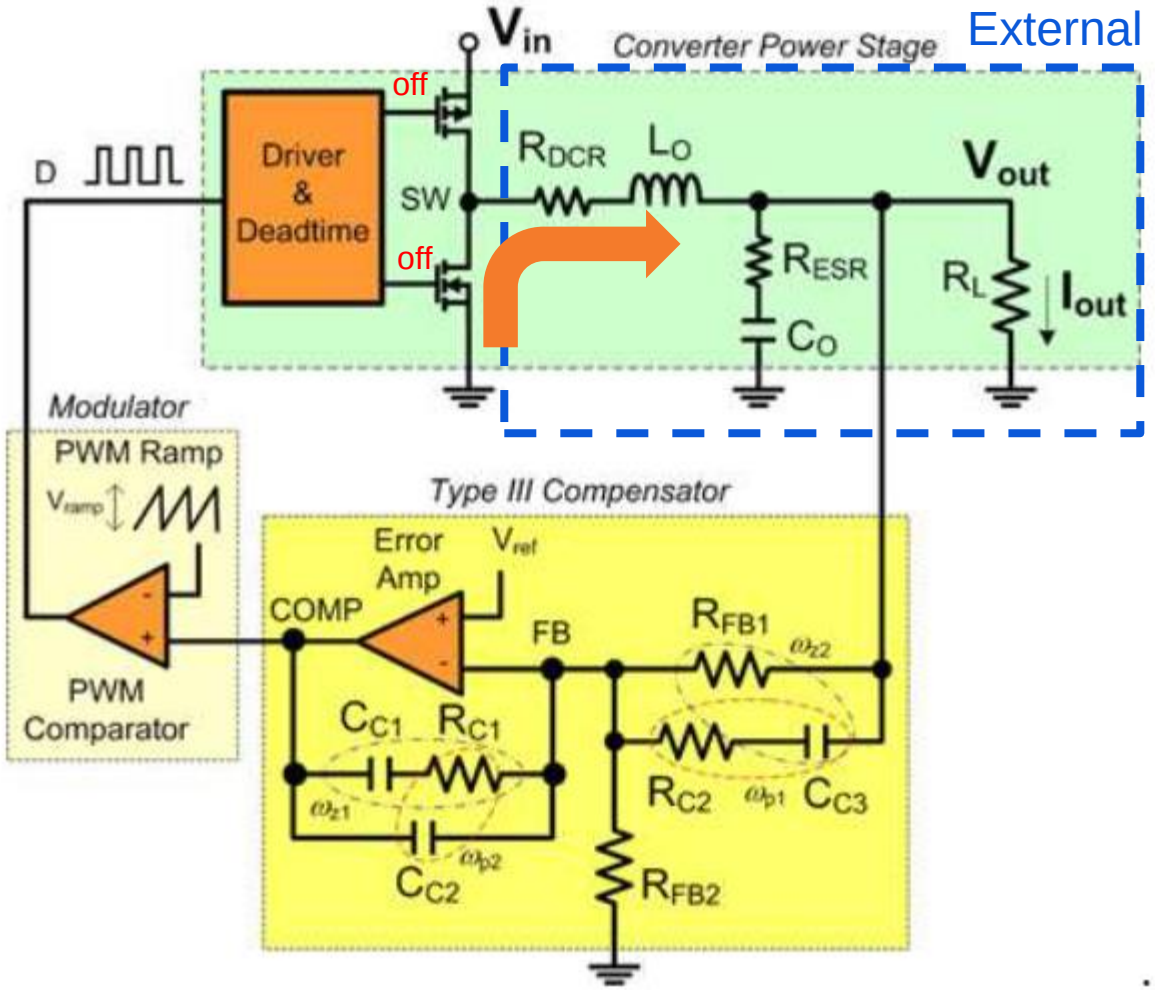
Dead Time of a converter

- Illustration of a voltage mode buck converter. Type III compensation

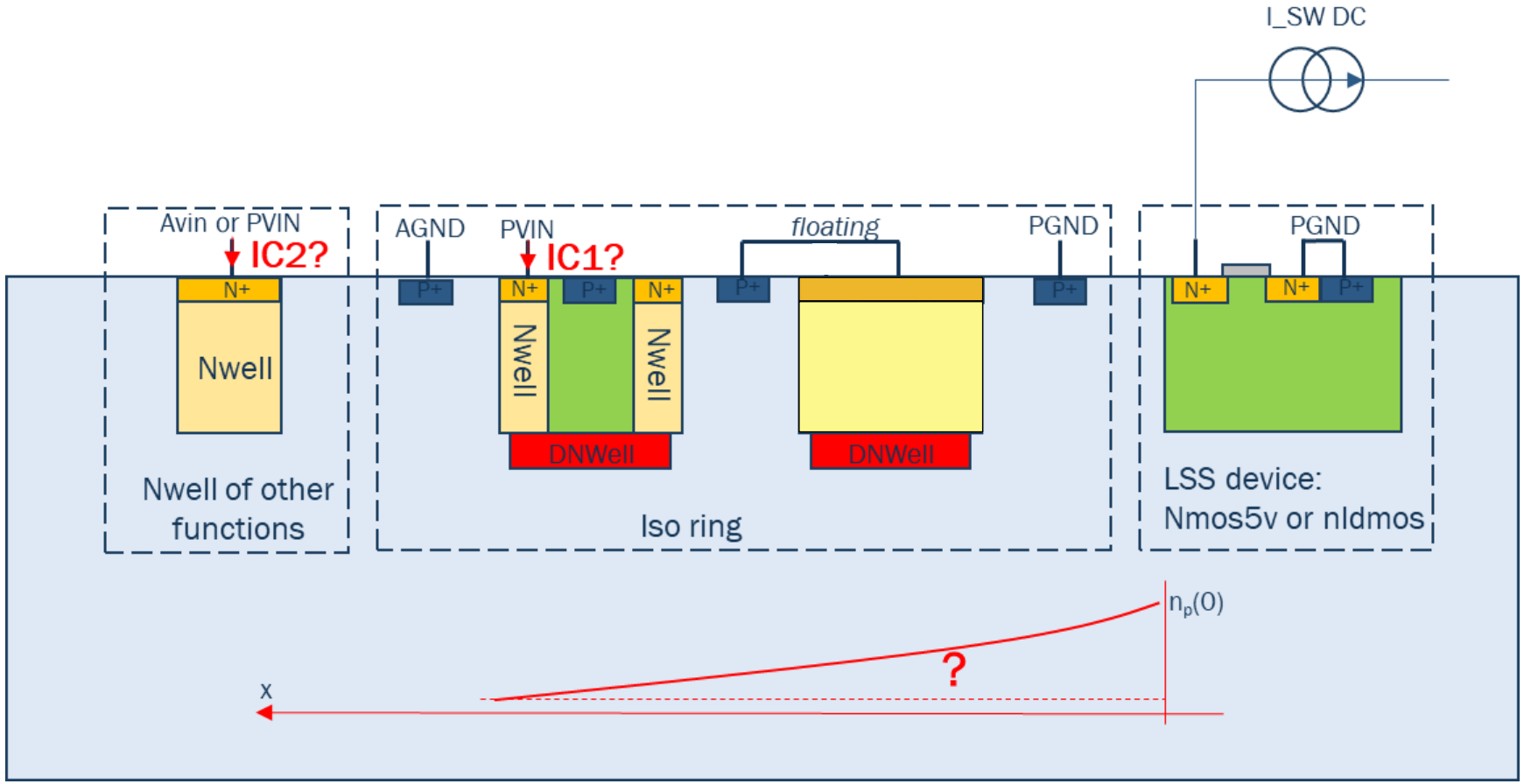


Dead Time:
When both high- and low- side switches are turned off.
However, current continues to flow out of switching node or the drain of low-side switch. That is electron injection into substrate as minority carriers, turning on parasitic bipolar.

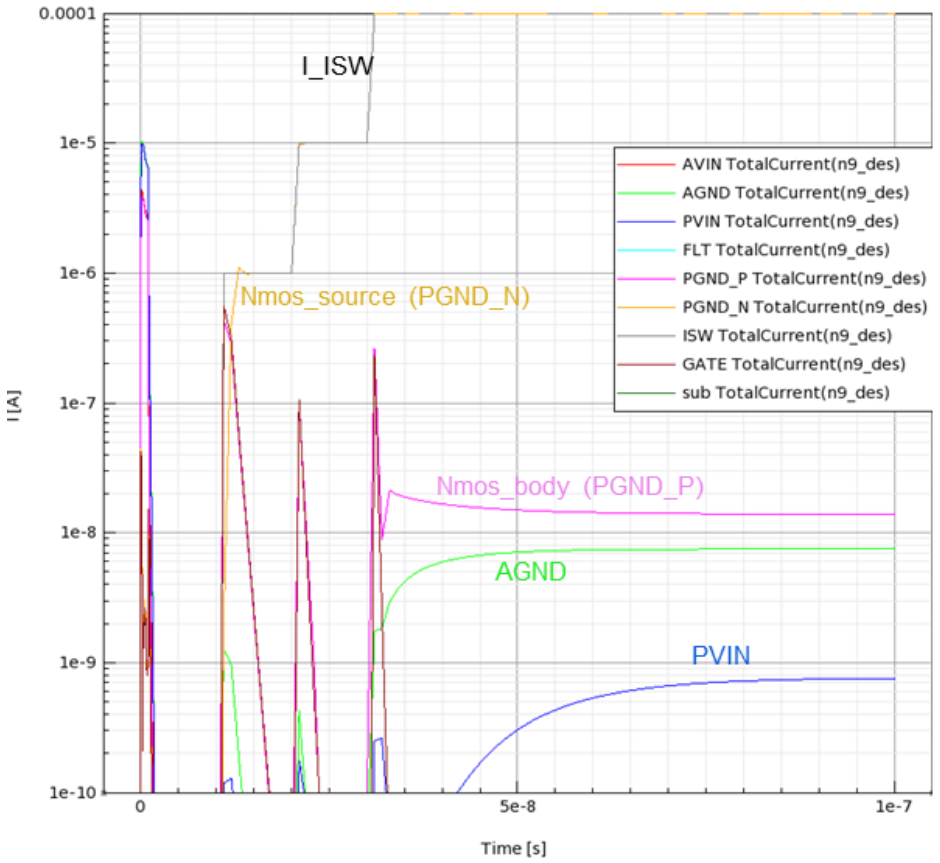
Concerns
- Power efficiency
- Disturb neighbor block function, e.g. a pmos bulk connected to its source

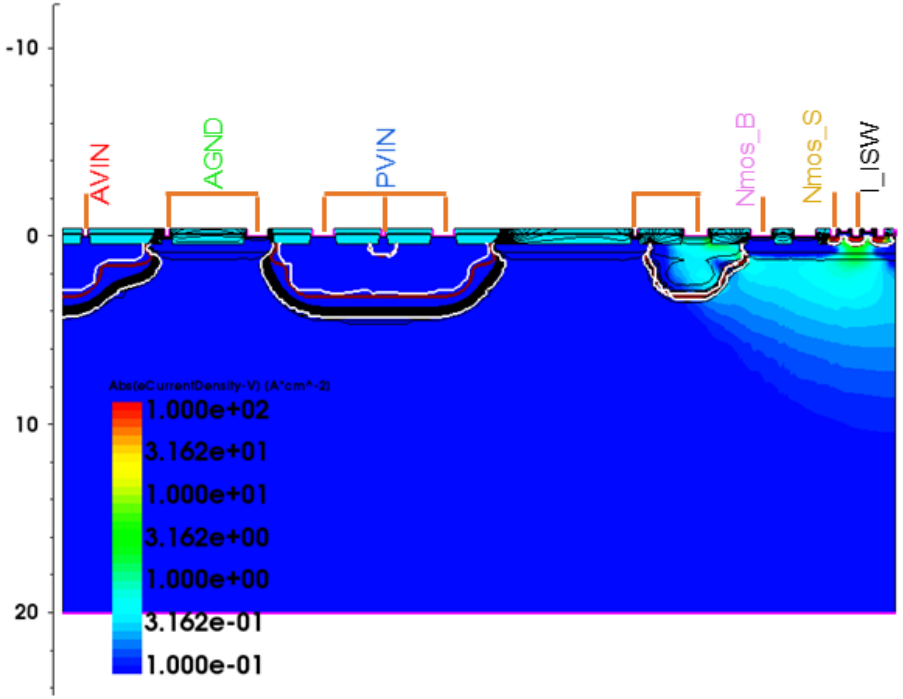
Courtesy of Olivier Causse

Multi-ring Active Analogic Protection (MAAP)



NMOS as LSS transistor case s-device simulation result

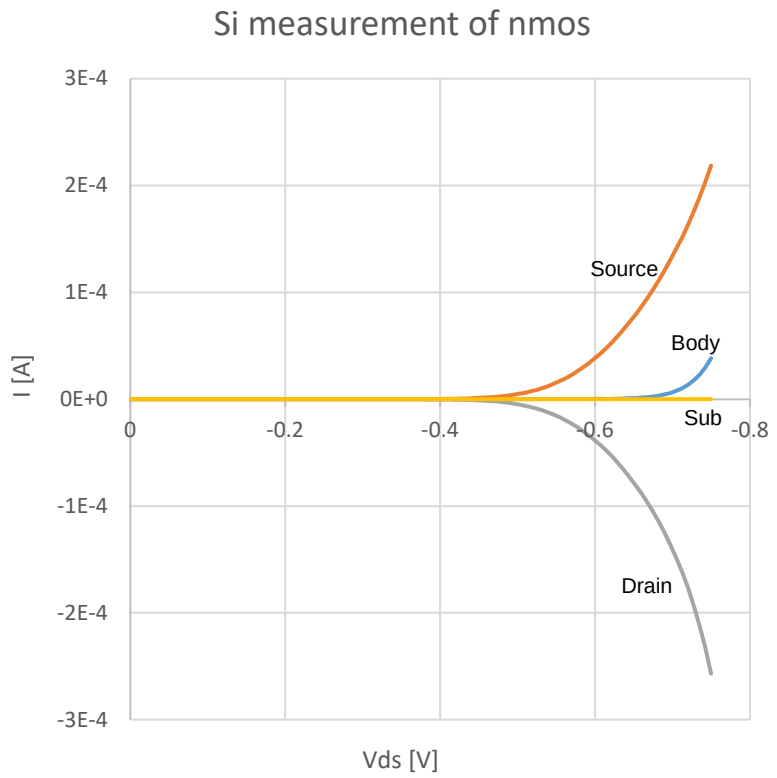




Current vs time waveforms for all terminals. Notice I_ISW and NMOS_source waveforms are overlapping at most of the time.

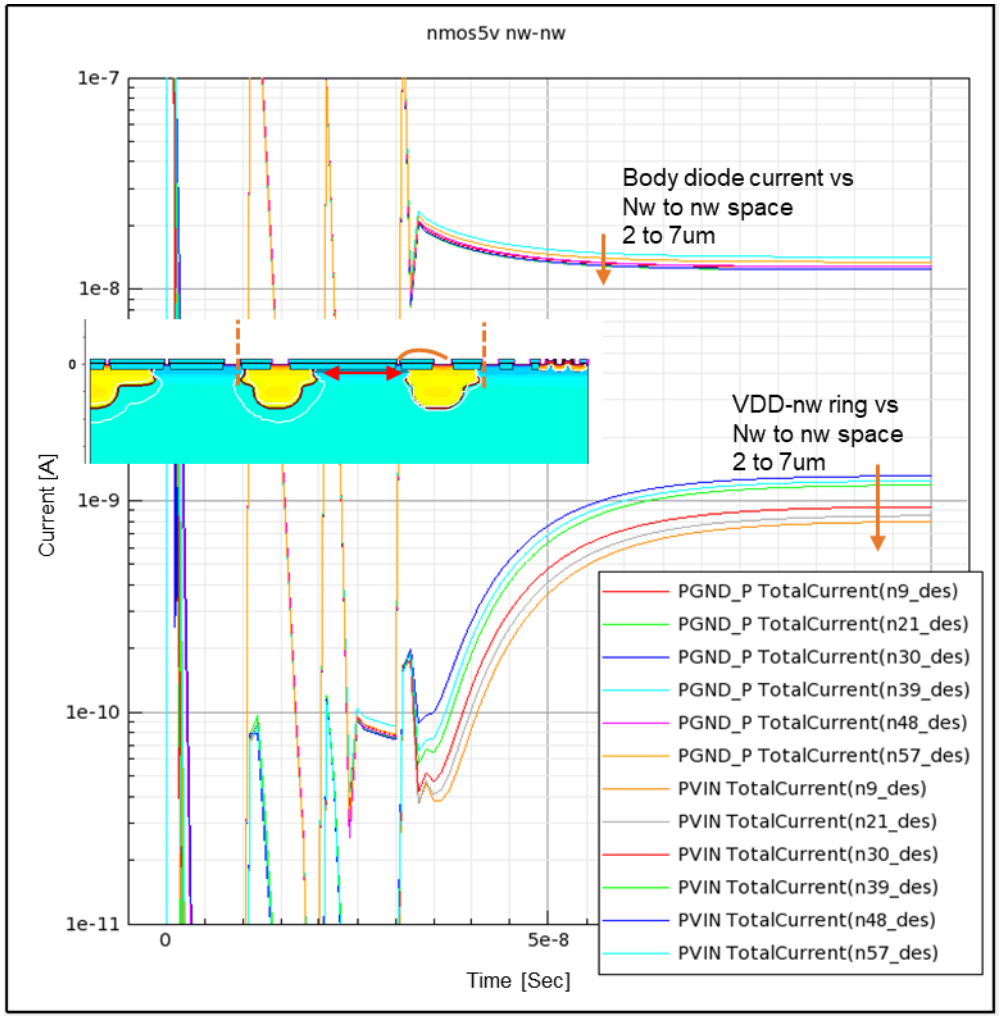
Structure cross-section view of electron current density color map & static potential contours with -1V~1V range, at 100ns time point.

NMOS device silicon measurement result



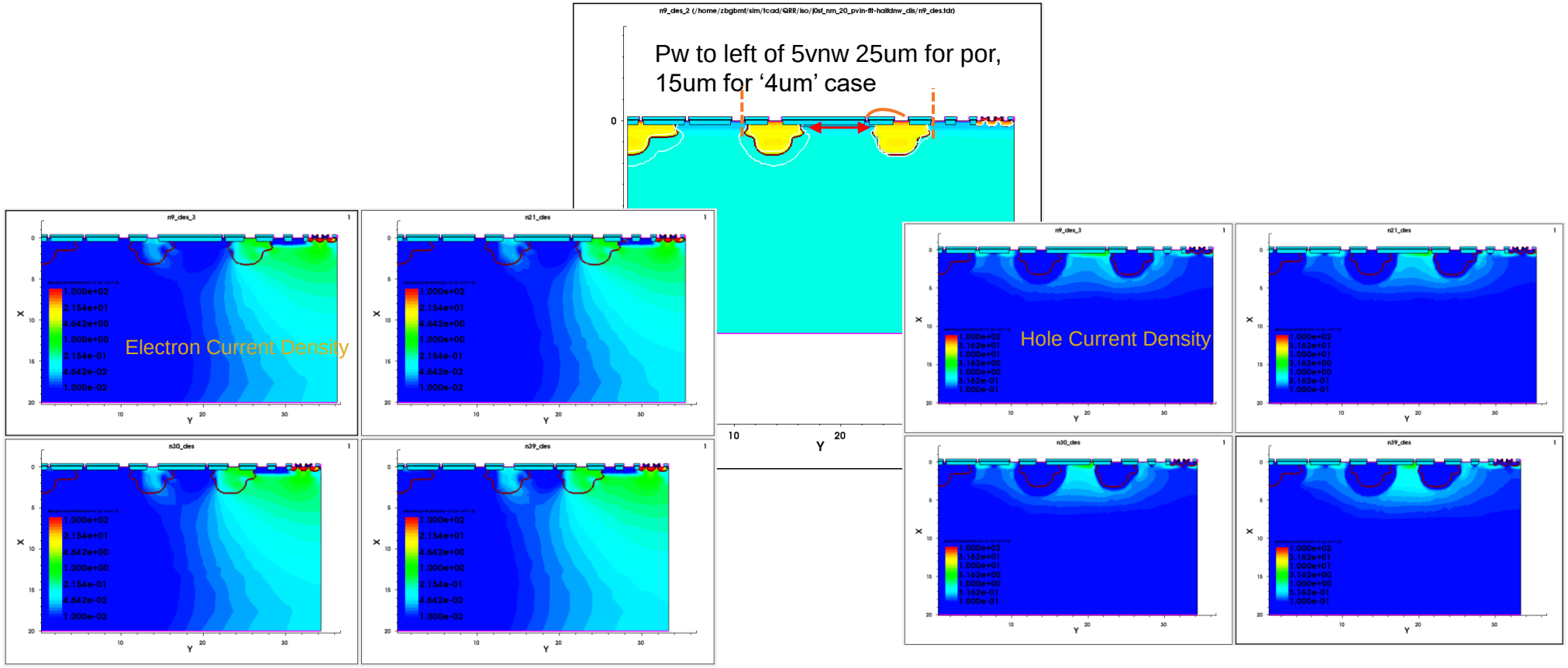
- Majority current from the Source through channel, instead of body diode.
- Drain voltage is swept from 0V to -0.75V, all other terminals grounded. Channel conduction occurs at much lower |Vds| value, before its high enough to turn on body diode.

NW to NW distance variations



Current vs time waveforms responses to NW to NW distance variations, from 2 µm to 7 µm, step by 1 µm. Vertical axis is zoomed in to focus on body diode and VDD-nw ring currents.

NW to NW distance variations



Conclusion

- NMOS/NLDMOS LSS dead-time minority carrier isolation is critical for Synchronous Step-down converter products both for reliability, power losses, and die size cost
- MAAP isolation ring design effectiveness with LSS NMOS or NLDMOS is evaluated using TCAD simulation
- instead of body diode, MOS channels conduct most of the current between source and drain, with minimum minority carrier injection to substrate
- high performance minority carrier isolation and significant die size cost reduction on the isolation ring region can be achieved at the same time

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