

High-density Nanoporous silicon decoupling capacitors

Murata Integrated Passive Solutions (MIS)

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Product Line Manager

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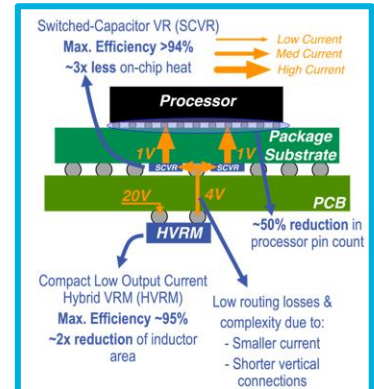
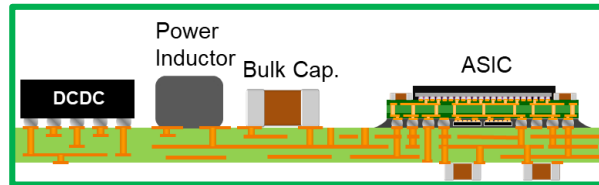


I. Introduction / Thoughts sharing

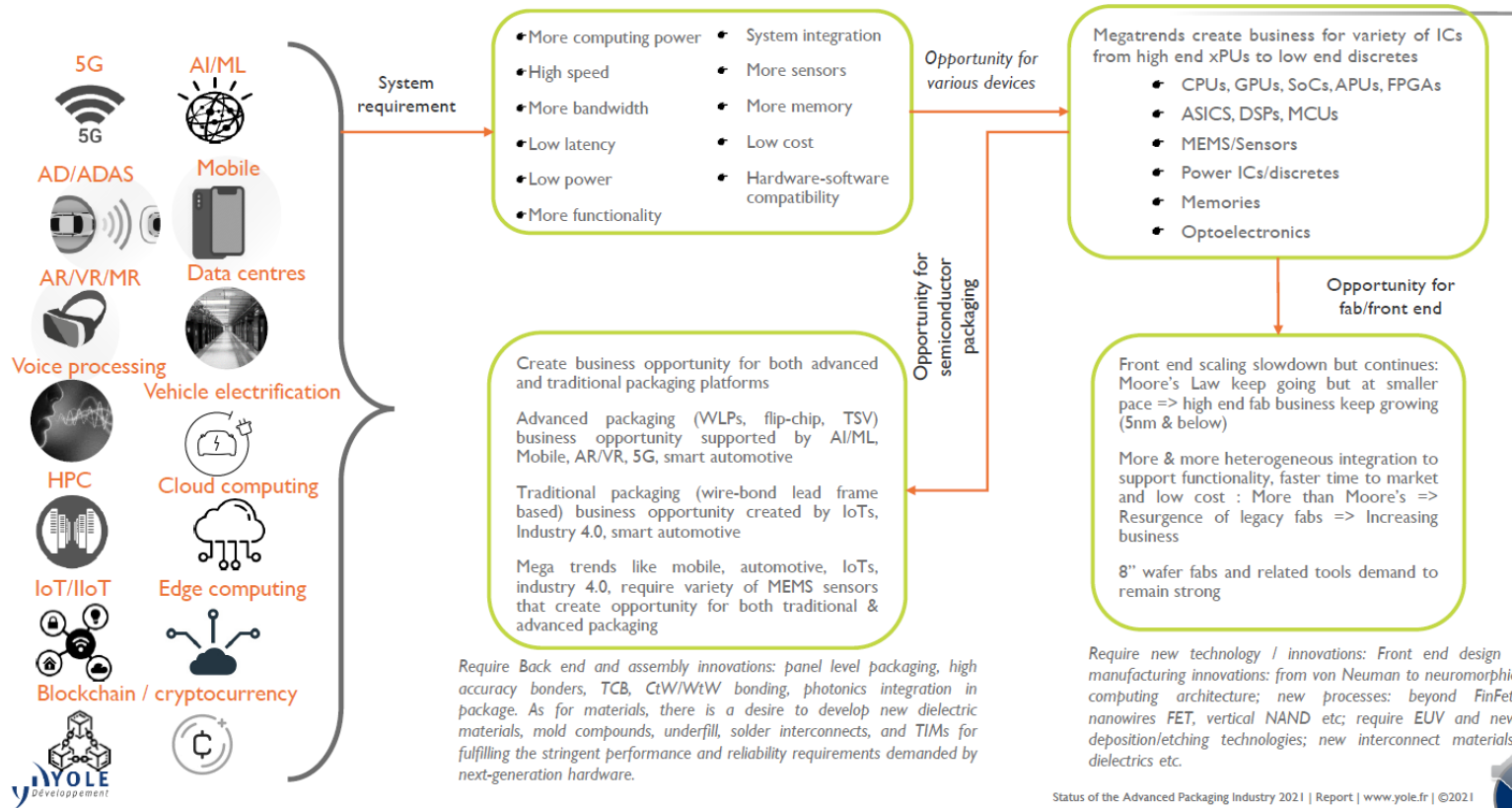
II. Silicon Capacitors: 5W (Where, Who, When, Why, What)

III. 3D Nanoporous Silicon capacitors for Power applications (PDN, iVR)

IV. Conclusion



I. Introduction

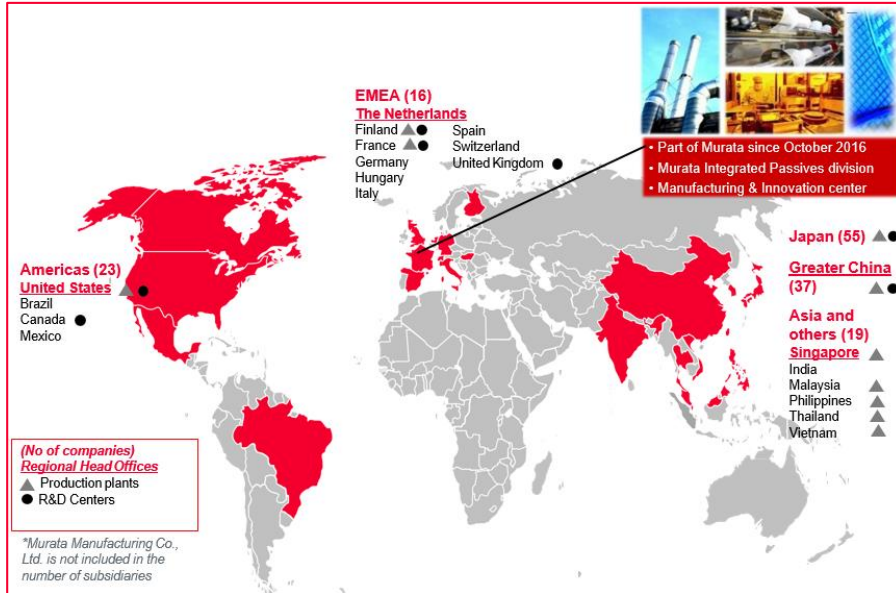


Status of the Advanced Packaging Industry 2021 | Report | www.yole.fr | ©2021

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Source: Yole Développement

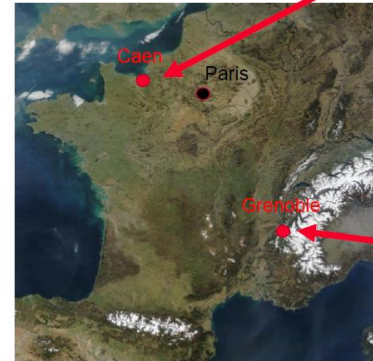
II. Murata Integrated Passive Solutions_ Where ?



• Part of Murata since October 2016
• Murata Integrated Passives division
• Manufacturing & Innovation center

Wafer foundry

- 6" clean room / 5000 m²
- Certified ISO 9001 / 14001 / 18001 and IATF 16949 for the Automotive market.



R&D center

- Integrated in Leti premise (Grenoble)
- 8" technologies
- Innovation for HD & HV portfolio



II. Silicon Capacitors technology_Who? When?

Long Lifetime, Down Sizing

High Capacitance GRM Series
(2.5V~100V, ~220uF)



Polymer Electrolysis ECAS Series
(2.5V~25V, ~470uF)



EDLC DMF Series
(~1000mF, 4.2V)



Low ESL LLL/LLD Series
(~4.3uF, 9.2uF)



Automotive Grade GCM Series
(ISO9001, AEC-Q200, TS16949)



Consumer

LED lighting, TV, Air conditioner
Smartphone, Tablet, Wearable

Healthcare

Imaging Therapy, Hearing Aid,
Clinic System

Safety Recognized DE Series

(13 countries Safety Approved, X2/Y1/Y2)



Industry

Factory Automation, PLC,
Inverter

Wind / PV Power
Generation, Oil/Gas System

Energy

SNUBBER (SHIZUKI) MIC-UV Series
(~1,600V, ~4uF)



High Power EVC Series
(~1,600V, ~4uF)



PA High Q GQM Series
(250V~500V, 1GHz~10GHz)



Ultra High Voltage DHS/DHK Series
(DC10~50kV, AC10~25kV)



DC-LINK (SHIZUKI) MEC-DL/HV Series
(~1,200V, ~1,600uF)



Optical Transceiver GMA/GMD Series
(Wire Bonding, Au Electrode)



High Voltage DHR Series
(6kV~10kV)



High Power Conversion

Ultra High Voltage, Communication

High Reliability

Metal Terminal KRM Series
(25V~1kV, ~100uF)



Implant Class D GCR/GCH Series
(ISO13485)



Embedded GRU/LLU Series
(110um~, Cu VIA Connection)



Ultra Small Size GRM01/02 Series
(008004, 01005)



Non Magnetic MA Series
(MRI application)



Multilayer RDE Series
(~220uF, ~2kV)



High Density
Miniaturization
Low profile
Low ESL



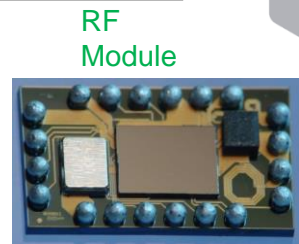
Low ESR
High Reliability
Mechanical strength
High Stability

Wrong choice of passives can impact and limit the final application

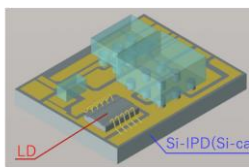
II. Silicon Capacitors technology_ Where?



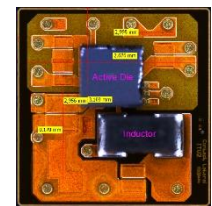
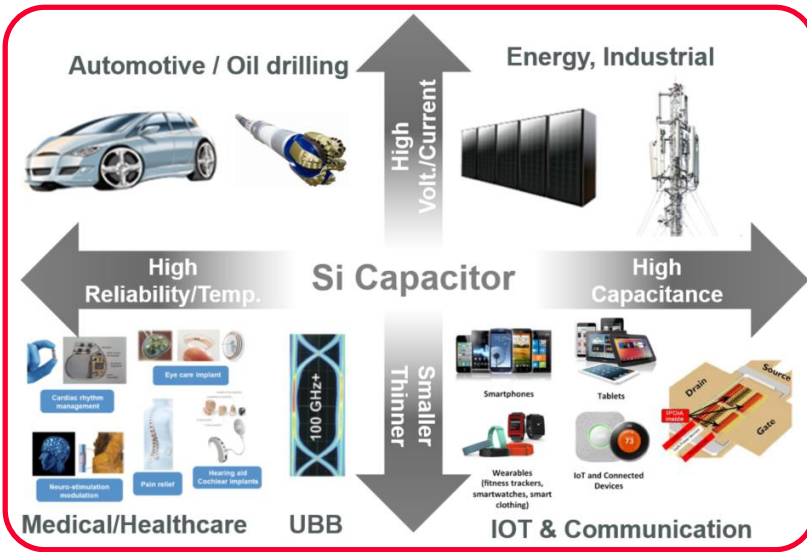
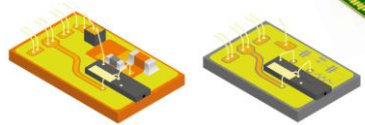
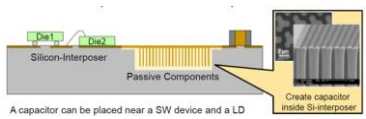
Optical transceivers



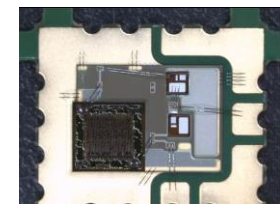
RF Module



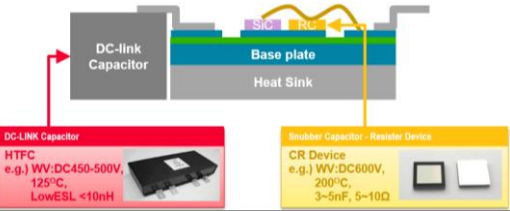
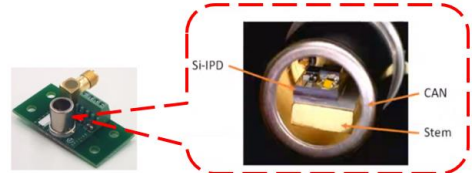
LiDAR Module
140W, <1ns pulse



DC-DC Converter
100MHz



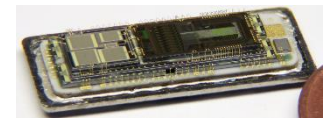
High voltage DC-DC Converter SiC /GaN



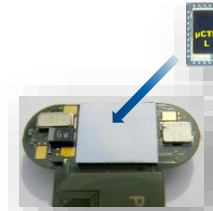
WBG power switching



Smart Lens



Neurostimulation module

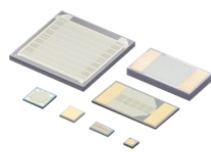
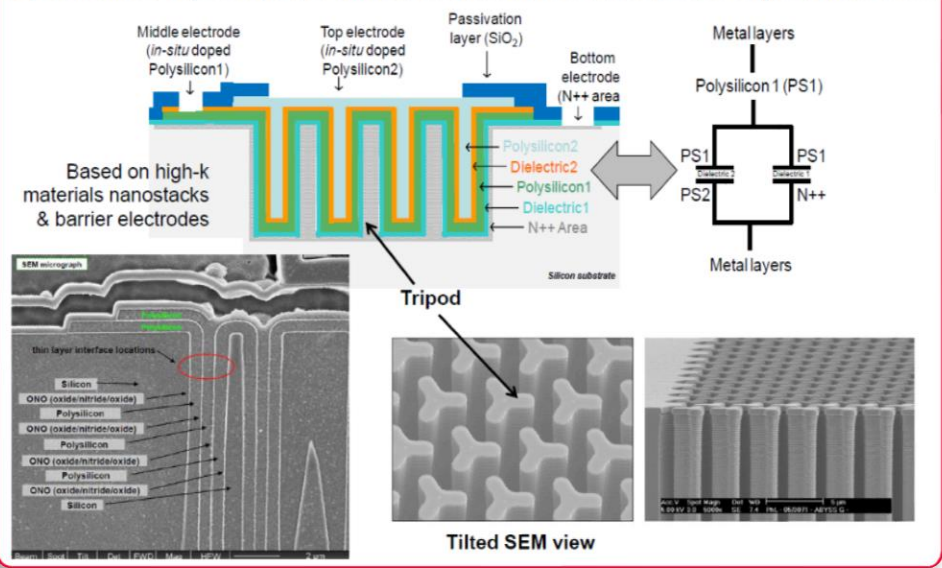


E-Pill






II. What's Silicon Capacitors Technology ?



2 parallelized capacitors in a MIMIM architecture to increase the capacitance value

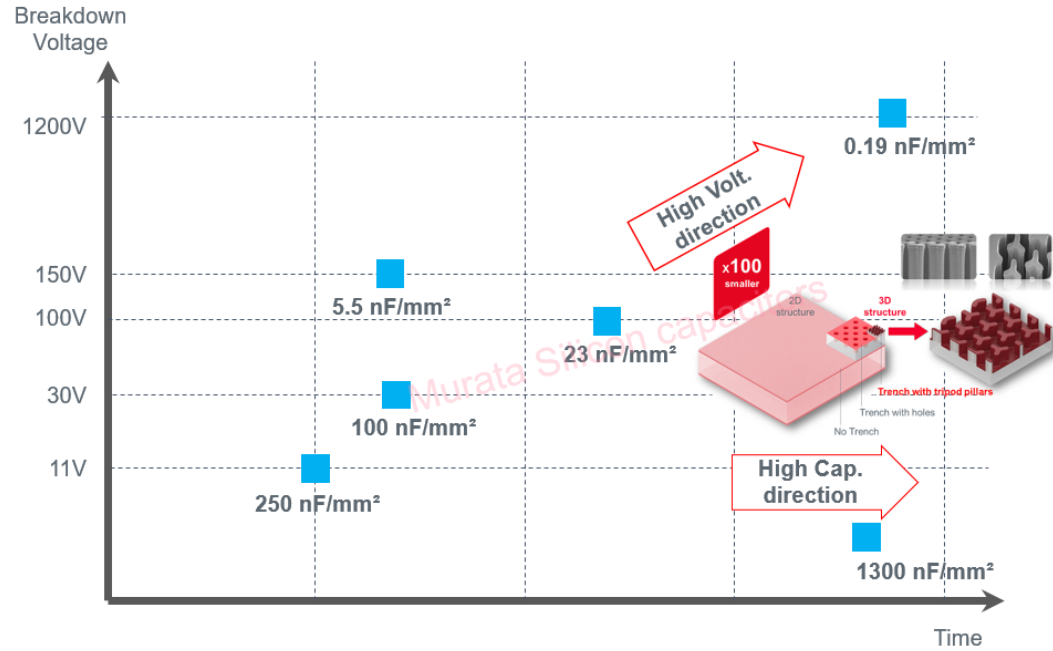
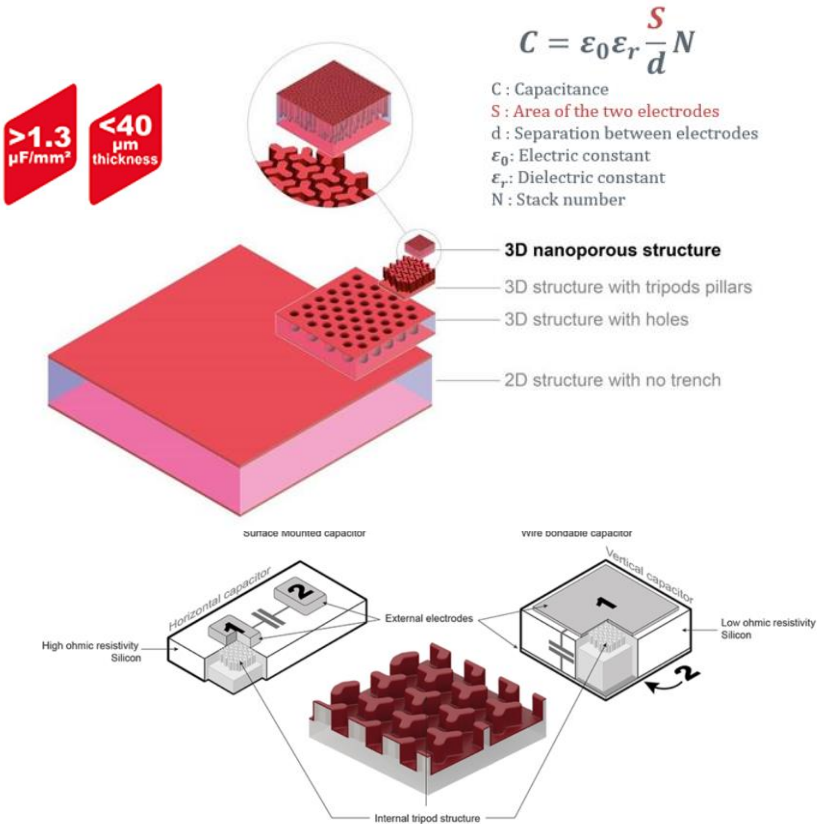


Silicon Capacitors

-  **High stability in temperature**
Up to **250°C** environments
-  **Signal stability over frequency**
Up to **110 GHz** applications
-  **Stability regarding voltage**
For **450 V** applications
-  **Stability over ageing**
Minimum lifetime of **10 years**
-  **Extreme low thickness**
Down to less than **50 μm**

- Murata is committed to a vision of developing innovative integrated Silicon capacitors to match the requirements and trends of SOC

II. What's Silicon Capacitors Technology ?

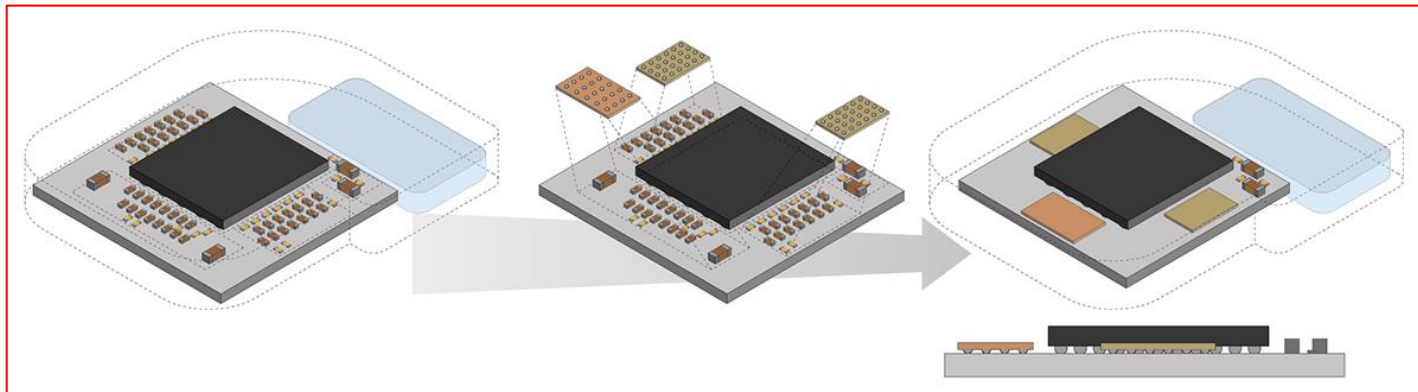


Silicon Capacitors extending MLCC portfolio

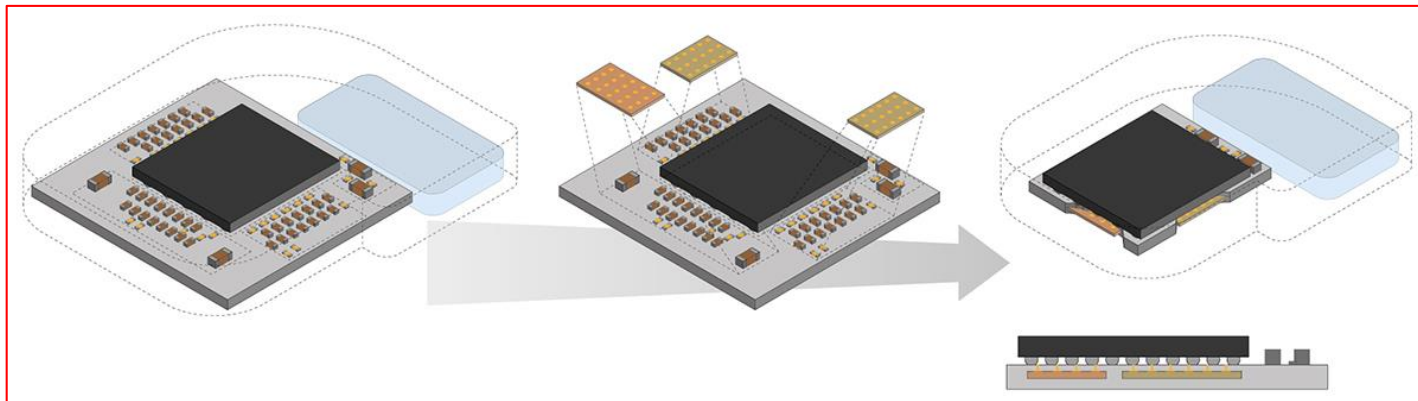
II. What's Silicon Capacitors Technology ?



Die Side



Land Side
or
Embedded

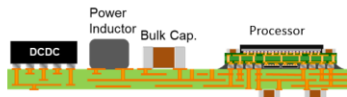


III. PDN_di/dt Mitigation

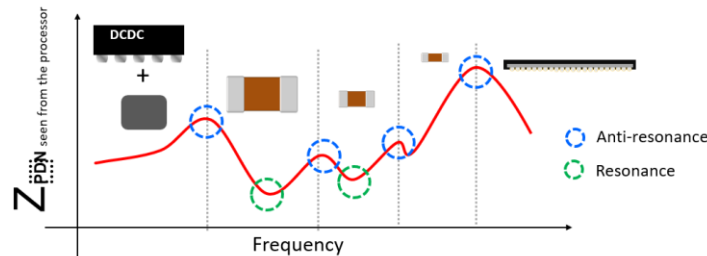
- Workloads exert excessive load transients and instability in the power supply network → variation in CPU activity may cause droop with steep slopes
- The di/dt events of CPUs induces voltage transients that need to be margined for, at the cost of power and performance
- Higher performance cores switch more current, inducing deeper droops. This impact is amplified at lower operating voltages as required by scaling trends

→ There is a need for an efficient PDN decoupling strategy

$$V(f) = \boxed{Z_{PDN}(f)} \times I(f)$$

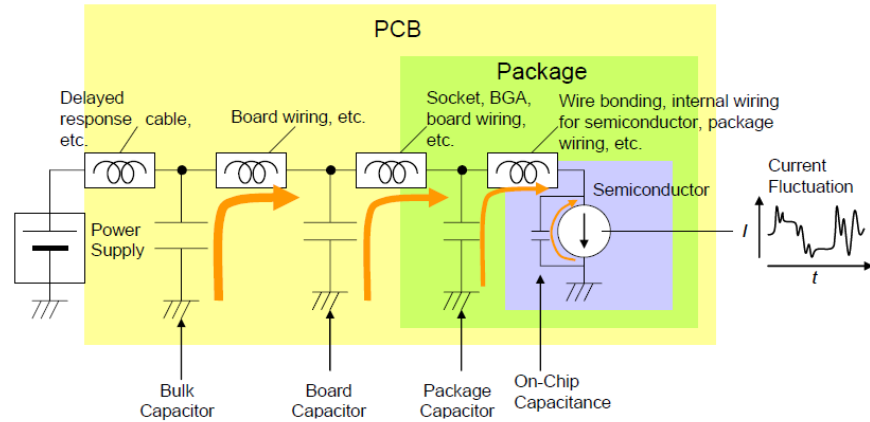
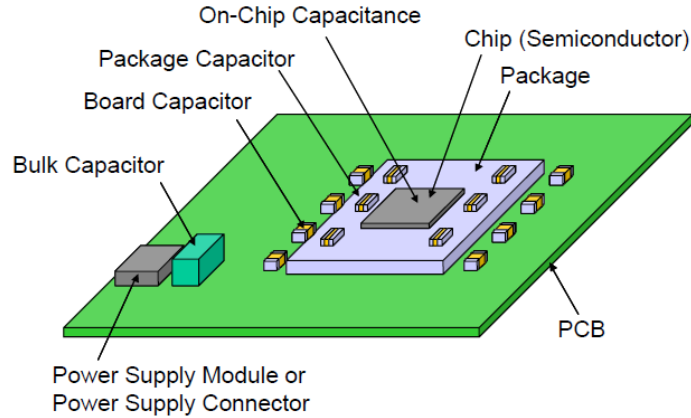


Vdd ↓ ! Idd ↑ ! Ztarg ↓ ↓

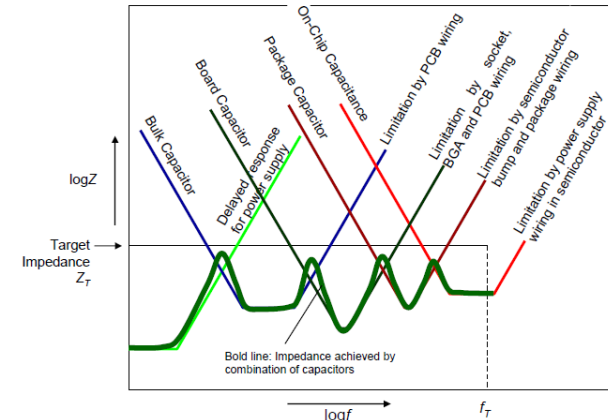


Need to take care of anti-resonance and resonance to mitigate voltage noise

III. PDN_Application



- Power supply impedance must be made small over a wide frequency range
- One capacitor cannot achieve the necessary impedance, multiple capacitors are positioned hierarchically to achieve the target power supply impedance
- Due to space constraints, on-chip capacitance is not enough to reduce impedance at high frequencies.



III. PDN_Trends and Requirements

Thickness



FOWLP / FOPLP

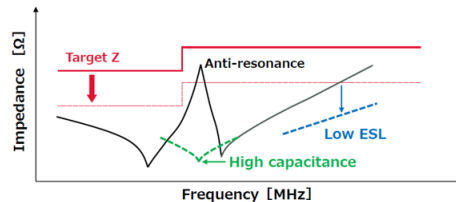
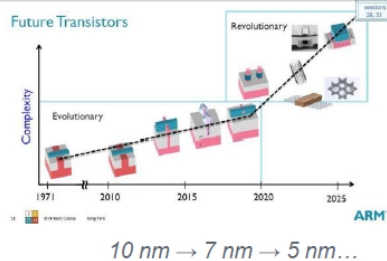
- Fine L/S (\rightarrow Fine BGA pitch)
- Low profile



Low profile capacitor is needed

ESL

Microfabrication of process \Rightarrow Lower target impedance



Low ESL capacitor is needed

General Trends for Mobile & HPC

- Higher functionality
- Scaling
- Increase in Power density

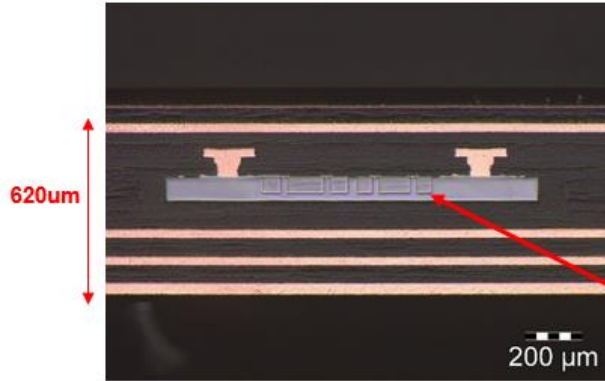
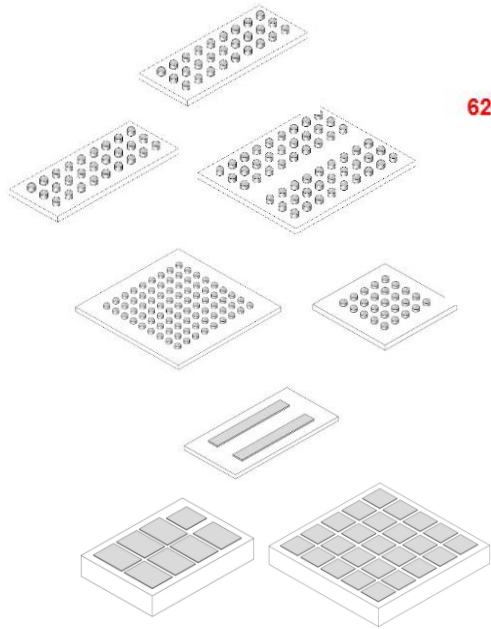
General requirements for PDN

- More stability & flat design
- Lower Z design at high frequency
- Lower Z design at anti-resonance

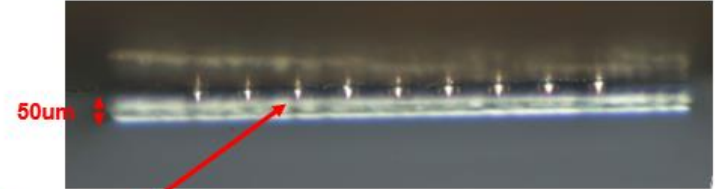
Needs for Capacitors

- Extreme Low ESL
- Extreme Low profile (Die, Terminal)
- High capacitance
- Adjustable ESR

III. PDN_Murata's UESL® family solutions



Embedded Si-cap



LSC Si-cap

3D Structure

Ultra Low ESL Silicon capacitor with:

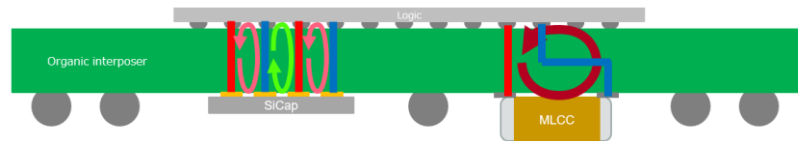
- State of the art density of $>1300 \text{ nF/mm}^2$ in Silicon
- $1 \mu\text{F}$ in ultra compact 0404 form factor
- Ultra-low ESL ($< 5 \text{ pH}$) and ESR ($< 5 \text{ m}\Omega$)
- $< 50 \mu\text{m}$ thickness
- Mechanical robustness

III. PDN_Benefits

Si-Caps help reducing ESL

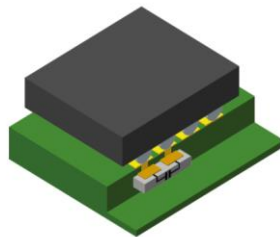
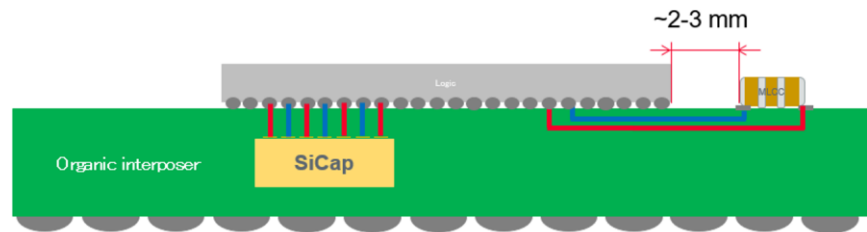
- **Landside packaging**

- Si-Caps intrinsic ESL is lower than MLCC
- Assembly ESL (parasitic) is reduced
 - Multi-terminals generate smaller current loop → lower ESL (shorter distance between pads)
 - Low-profile enables integration closer to IC



- **Embedded packaging**

- Ability to reduce substrate X/Y size

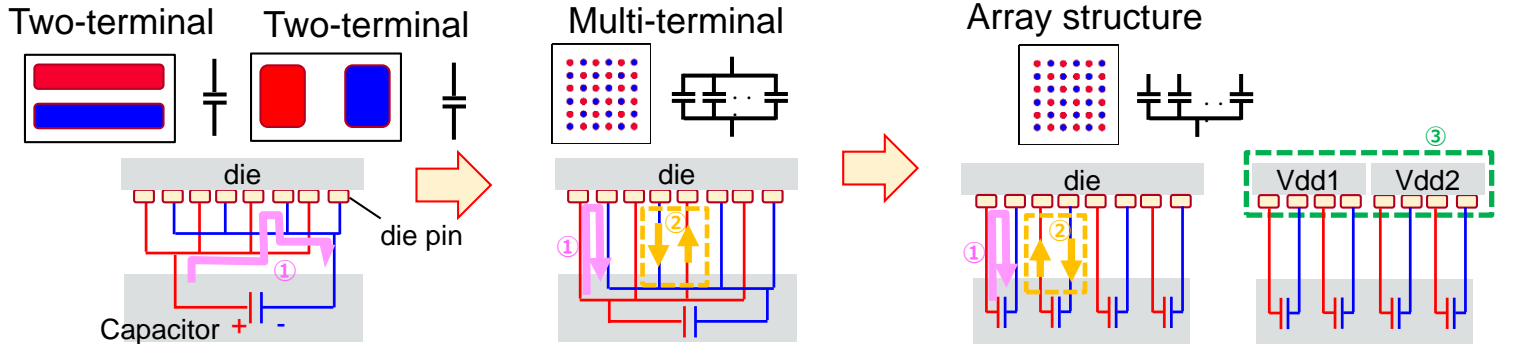


Source: <https://www.murata.com/en-eu/products/capacitor/siliconcapacitors/overview/medical>

Decoupling cap	Parasitic from assembly	Cap intrinsic ESL	Conclusion
MLCC die-side	High ESL high distance - Underfill	High ESL	Standard
SiCap embedded	Low ESL close to IC	Low ESL Multi-terminals Adjacent opposite loops	Improvement

III. PDN_Multi-terminal and array structure

Multi-terminal is important to get low ESL.
Array structure offers high flexibility for PDN design

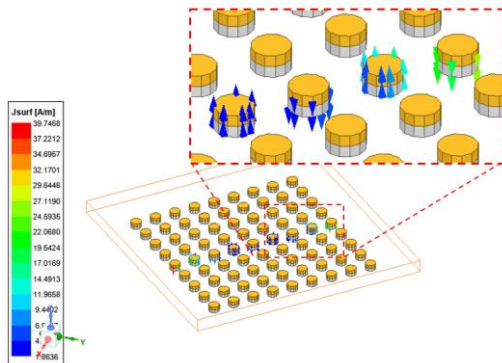


current path —
 current direction —

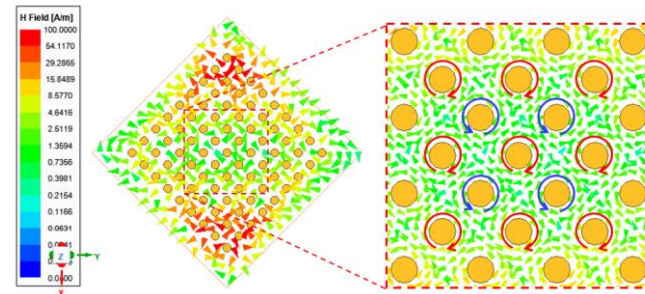
- Loop decrease(①)
 - Counteract electromagnetic wave(②)
- Low ESL in capacitor**
Low inductance of wire

- Loop decrease(①)
 - Counteract electromagnetic wave(②)
- Low ESL in capacitor**
Low inductance in wire
 • Capability to connect different power domains(③)
 →Flexibility of AP design

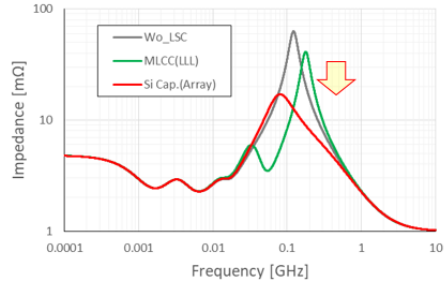
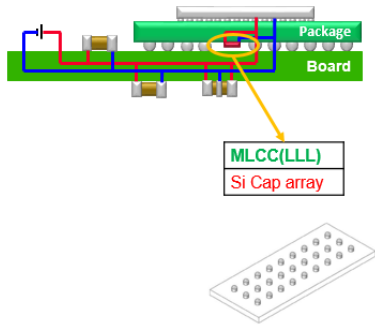
Surface Current distribution @ 1GHz



Magnetic field distribution @ 1GHz



III. PDN_Si-caps improve system performance



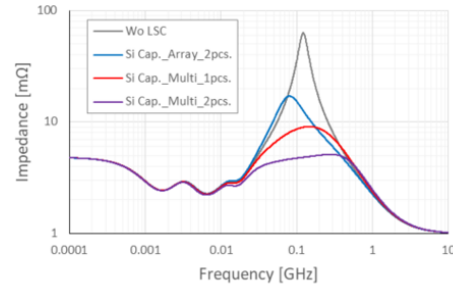
	Z_{peak} (mΩ)
Wo LSC	62.7
MLCC(LLL)	41.2
Si Cap.(Array)	17.0

-24.2 mΩ

- Abrupt changes in processor activity induce large current transients in the power delivery network
- There is a need to reduce losses → provide better and more granular regulation to the processor cores



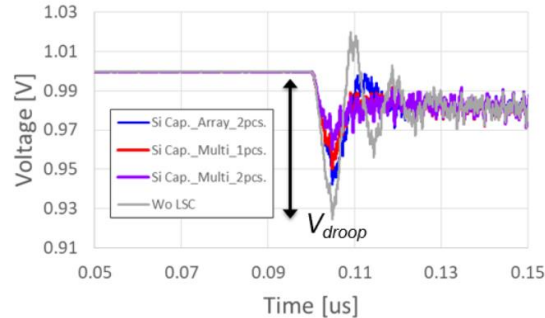
Z_{peak} : anti-resonance between Chip and Board



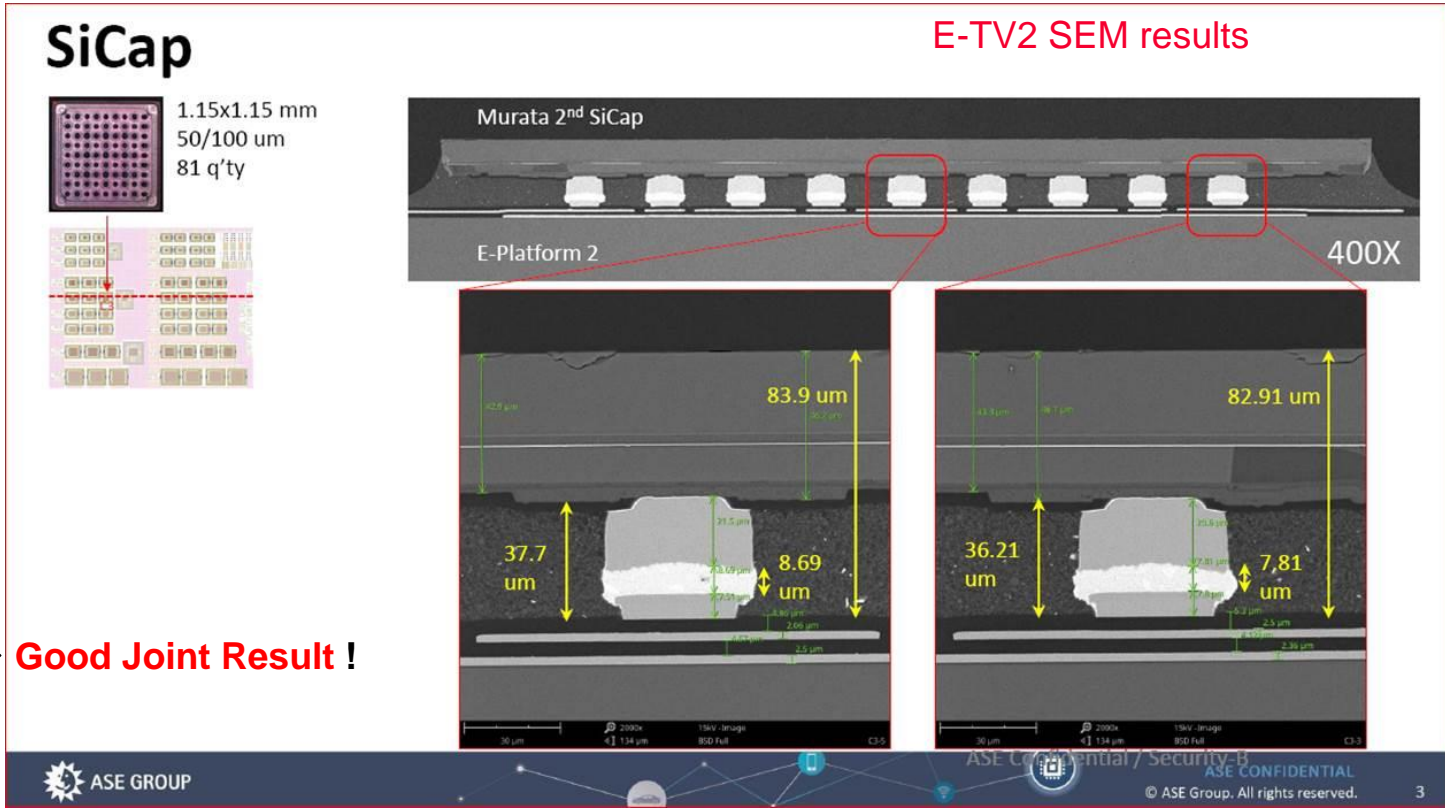
	Z_{peak} (mΩ)	Improvement rate (%)
Wo LSC	62.3	
Si Cap. ×2 pcs.	17.0	-72.7%
Si Cap. ×1pcs.	9.1	-85.4%
Si Cap. ×2pcs.	5.1	-91.8%

* Wo LSC = Without Land Side Capacitor
* In the case, we connect Si Cap. (Array) to same power line

- Z_{peak} is reduced by mounting LSC.

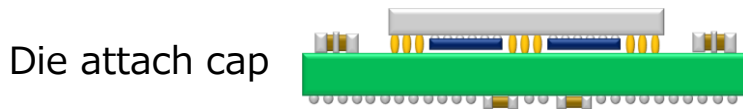
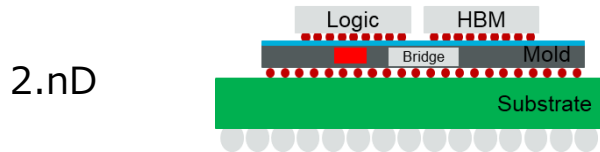


III. PDN_Assembly evaluation



Courtesy of ASE R&D Team

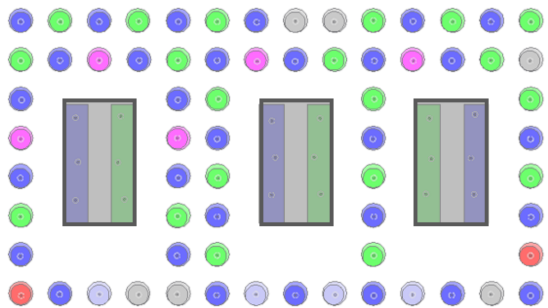
III. PDN_Advanced packaging



Power Integrity can be improved using specific cap:

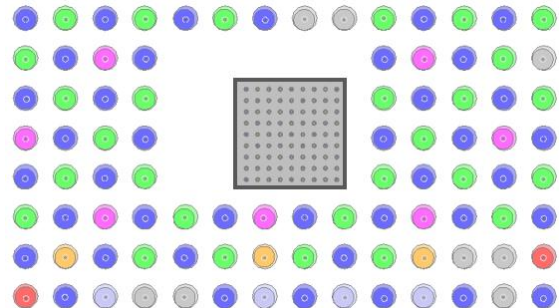
- DC~1MHz Standard (High capacitance)
- 0.1 MHz Multi-terminal (Low inductance)
- 25 MHz Package Cap (Thin and Embedded cap)
- 100s MHz Si Multi-terminal 3D cap

45 depopulated BGA



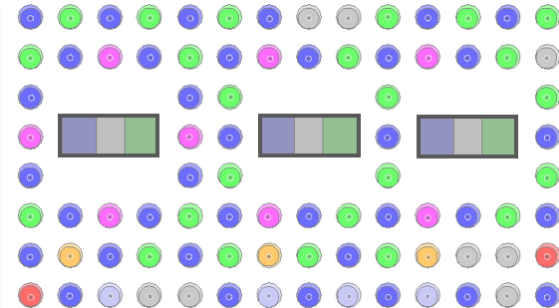
LLLx 3 pcs (0204)

20 depopulated BGA



0404 Si-cap x1pcs

27 depopulated BGA



GRM x3 (0402)

III. iVR_Traditional Power Delivery

UC San Diego

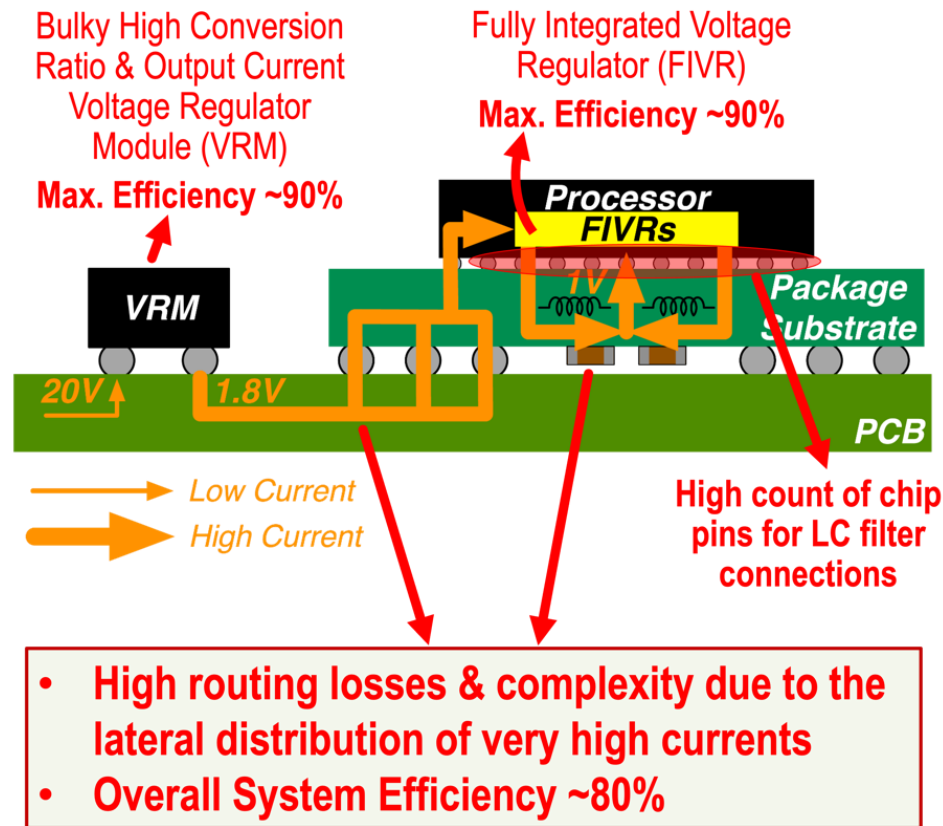
Prof. Hanh-Phuc Le and his team

iPower3Es integrated Power Electronics and Energy-Efficient Systems Lab
Create Miniaturized Power for All

SRC Semiconductor Research Corporation
Global Research Collaboration

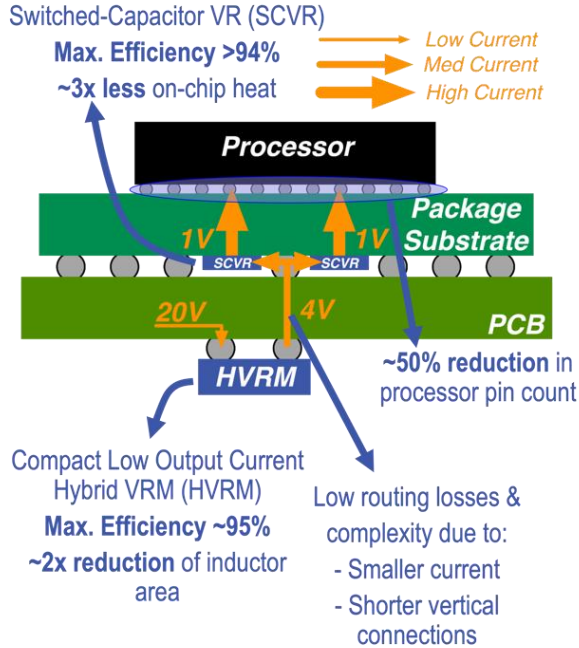
Qualcomm

3D-PEIM
3D Power Electronics Integration and Manufacturing



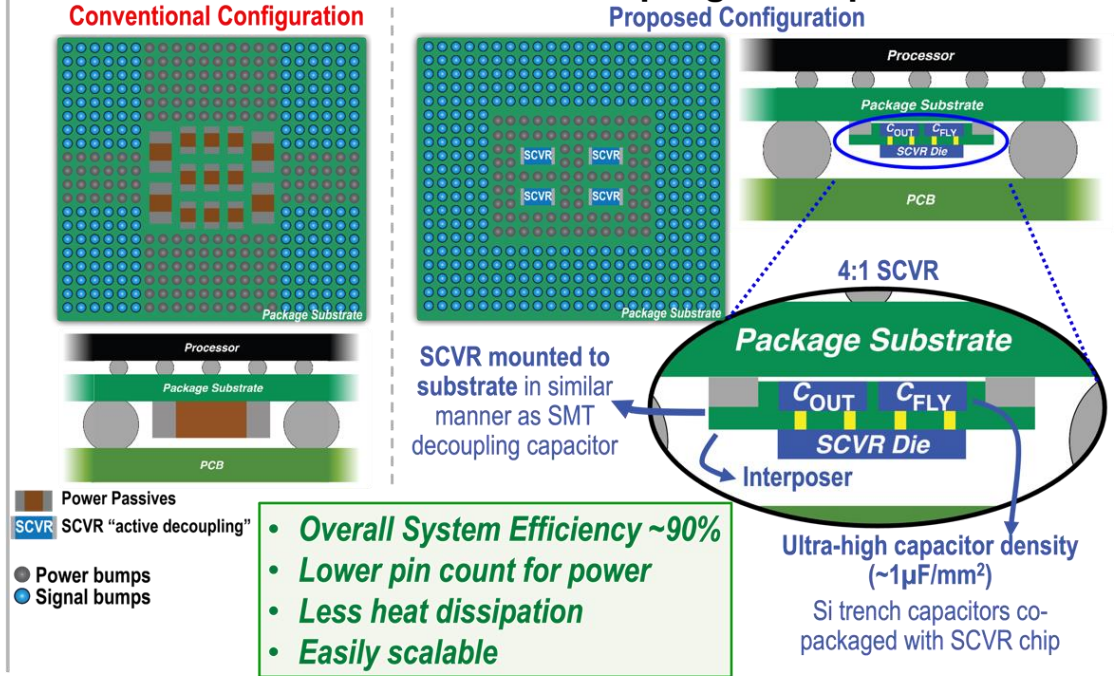
III. iVR_ Approach based on Two-Stage Vertical PD and Management with Heterogeneous 3D Implementation

Vertical PD Architecture



- ~2x reduction in package PDM pins
- 4x interconnect loss reduction;
- ~1.5x increase in available data IO pins.

SCVR "Active" Decoupling Concept



Confidential – Unpublished materials!

UC San Diego

Prof. Hanh-Phuc Le and his team

Unpublished Materials
Will be published at
ISSCC Feb. 2023

Confidential – Unpublished materials!

Vertical Power Delivery with Heterogenous Integration

- New circuit topology and control
- Switched capacitor for the last stage
- Integrated passive devices (IPDs)
- $>1 \text{ uF/mm}^2$
- Silicon interposer for packaging
- Target: 2 A/mm^2
- **87% total efficiency, with 94% for HVRM and ~93% for SCVR**
- Accepted to ISSCC 2023

VI. Conclusion_On-package Si-cap for CPU

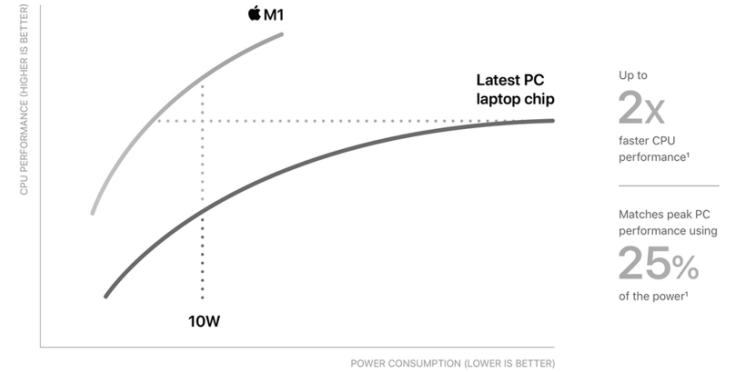
Macbook Pro 2020



M1 Chip



CPU performance vs. power

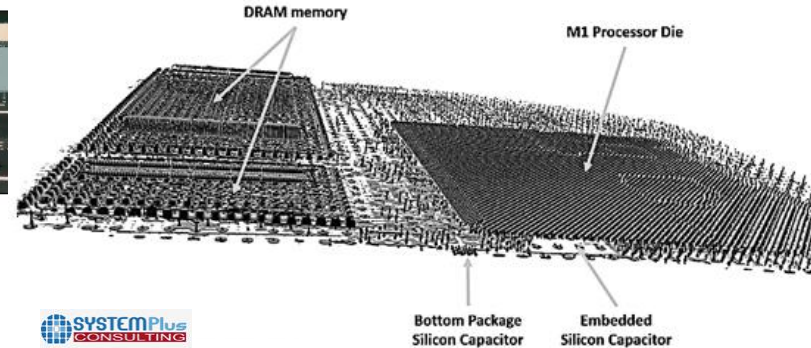


4 Land Side + 6 Embedded Silicon capacitors

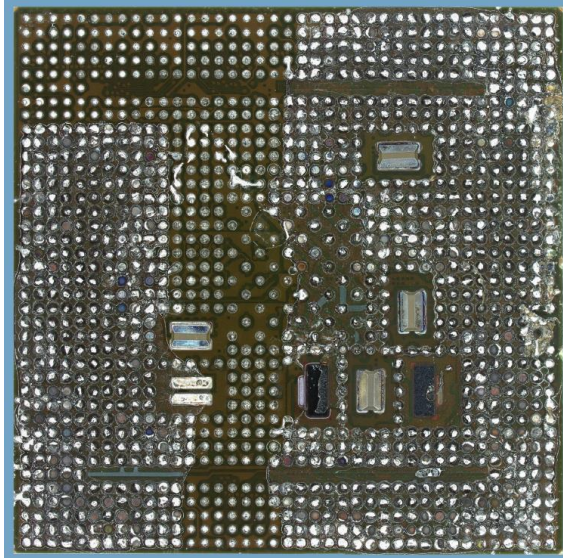


M1 SoC Package Cross Section 1
©2021 by System Plus Consulting

Embedded Silicon capacitor



VI. Conclusion_ On package Si-cap for APU



GS22_APU Bottom view

Galaxy S22 | S22+



Source:  SYSTEMPlus
CONSULTING

Silicon capacitors → enabling innovation and push the limits

Thanks a lot for your time and attention!

Contact: mohamed.jatlaoui@murata.com

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www.murata.com



cutt.ly/sicapweb

Silicon Capacitors **Catalog**



cutt.ly/sicapcatalog