Manufacturing Challenges and Qualification for 3D Packages

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SkyWater Technology

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You've Seen the Headlines…

Intel Announces Next US Site with Landmark Investment in Ohio

Intel will invest more than $20 billion to build two new factories and to establish a new epicenter for advanced chipmaking in the Midwest.

TSMC earmarks record $44 billion for chip manufacturing expansion in 2022

An almost 50 percent increase

Micron to invest $40 billion in U.S. chip manufacturing

Samsung lays out plans for a $200 billion expansion of chip plants in Central Texas

GlobalFoundries to seek CHIPS Act funds for Vermont chip plant

SkyWater Plans to Build Advanced $1.8B Semiconductor Manufacturing Facility in Partnership with the State of Indiana and Purdue University

Why Biden's plan to boost semiconductor chip manufacturing in the U.S. is so critical

Congress passes bill boosting US semiconductor production

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The Decline of U.S. Semiconductor Manufacturing

- The U.S. contribution to the global semiconductor manufacturing capacity has fallen from 37% in 1990 to 12% today
- Many governments have invested heavily to support the growth of the semiconductor industry in their countries, resulting in much of the total global manufacturing capacity now residing in Asia
  - This includes much of the “leading edge” technologies in CMOS device fabrication as well as advanced packaging capabilities
- While the COVID pandemic exposed some of the vulnerabilities of the existing semiconductor supply chain, there has been concern for even longer over U.S. ability to maintain the security and technological superiority of its electronic systems

A pervasive issue with far reaching economic consequences

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A Ubiquitous Need for a Stable and Secure Supply Chain

Automotive

Banking

Consumer

Industrial

Utilities

Cloud & Big Data

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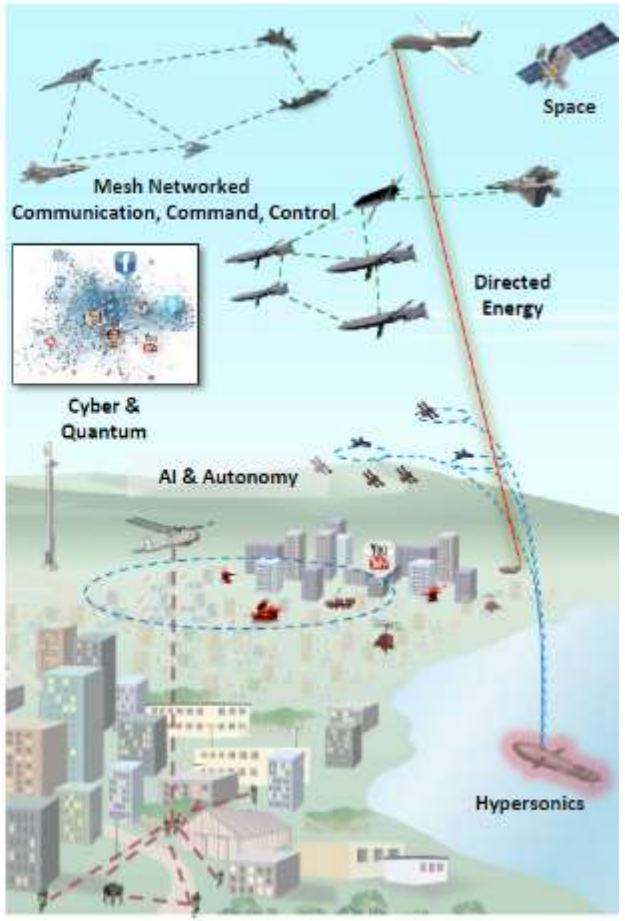
Defense and National Security Needs

- Continued reliance on non-U.S. microelectronics creates supply and security risks
- Volume requirements for these applications are significantly smaller than commercial markets
- Establishing security requirements within existing commercial providers is often not feasible

Dependency on Advanced Microelectronics Technology

- **Cyber & Quantum**
  - >1000x performance enhancement and efficiency for real-time ID/processing/response/security
- **Mesh Networked C3**
  - Open and distributed architecture to enable local processing of raw data on the battlefield
  - Adaptive processing for multi-antennas and frequencies for robust comm. and radar systems
- **Artificial Intelligence and Autonomy**
  - Need vision, semantic, and navigation processing for high-performance imagers and navigation
- **Directed Energy**
  - Advanced Imagers, optoelectronic technology, signal processing and control systems, spectral awareness
- **Space & Hypersonics**
  - Significant increases in rad-hard on-board sensor processing, communications, targeting, controls



NDIA Electronics Division Meeting
February 2019

Distribution Statement A: Approved for public release. Distribution is unlimited.

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Source: DoD Trusted and Assured Microelectronics Summary, Dr. Jeremy Muldavin, NDIA Electronics Division Annual Meeting, February 2019

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The Impact on Packaging in the U.S.

- Current estimates put the U.S. contribution to global semiconductor packaging at 2-3%
- None of the major OSAT companies have manufacturing operations in the U.S., though many have engineering, sales, and management operations here
- Several U.S. companies have prototype-to-low volume capabilities in several advanced packaging and heterogeneous integration (AP & HI) technologies supported by both government and commercial business
- While a majority of the $50B+ CHIPS funding will go to support front-end device fabrication manufacturing, a significant effort will be focused on the development of AP & HI manufacturing capabilities that are crucial to next-generation microsystems

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The Impact on Packaging in the U.S

- Two main program initiatives will be established under CHIPS that will impact U.S. packaging:
  - The Dept. of Commerce is to establish the National Semiconductor Technology Center (NSTC), a public-private consortium to support R&D and prototyping for advanced semiconductor technologies
  - NIST is developing a National Advanced Packaging Manufacturing Program (NAPMP), with directive to establish up to three Manufacturing USA institutes
- The CHIPS Act provides $2B for the NSTC and $2.5B for the NAPMP in the first year with an additional $6B in total for these initiatives in the subsequent 4 years
- A tremendous amount of preparatory activity has been taking place over the past year to prepare and plan for this effort
  - Dept. of Commerce received over 200 responses to a request for how these funds would best be used to establish U.S. manufacturing capabilities
  - Organizations like the ASIC Coalition have brought together companies, universities, and national labs to create a long-term plan and other similar organizations are also working along the same lines

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The Broad Scope of the Advanced Packaging Ecosystem

Design
- EDA software
- Multi-physics modeling

Substrates
- PCB
- HD laminates
- Ceramic
- Si & glass interposer

Physical Interconnect
- WLCSP
- C4 bumping
- Cu pillar
- Direct/hybrid bonding

Backend Processes
- Wafer thinning
- Dicing & singulation
- Temp. bond/debond

Assembly
- Flip chip
- TCB
- Direct/hybrid bonding
- 2.5D & 3D HI
- FOWLP
- SMT

Testing
- Wafer level
- Module level
- Reliability
- COTS upscreen

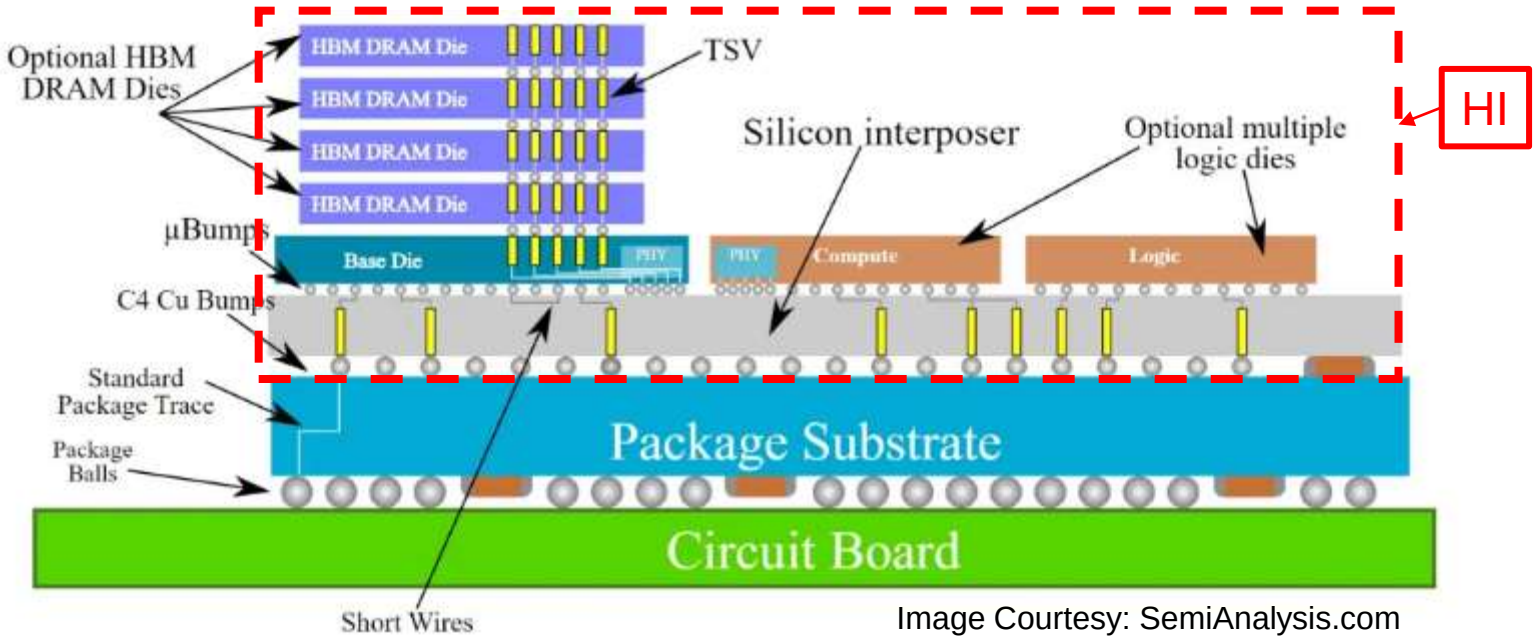

Image Courtesy: SemiAnalysis.com

- Materials
- Equipment
- Security Protocols
- Workforce

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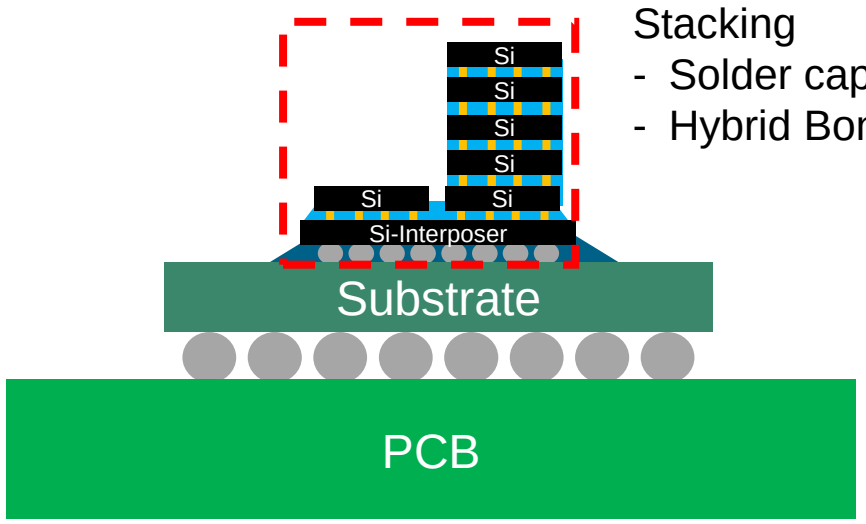
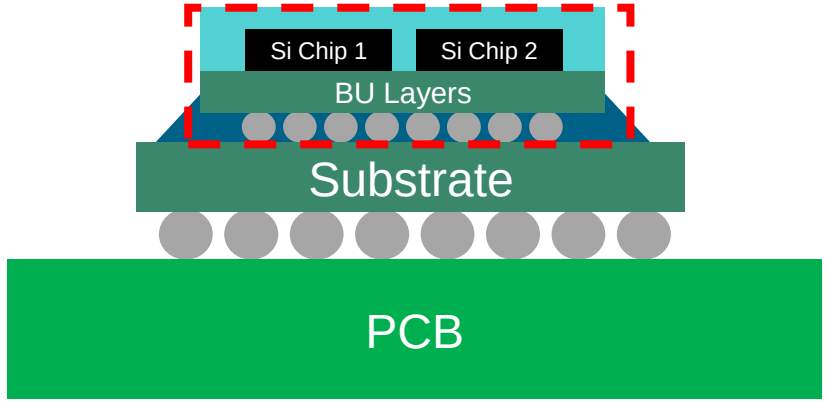
Pathways to Heterogeneous Integration



Stacking
- Solder capped Cu-pillars
- Hybrid Bonding

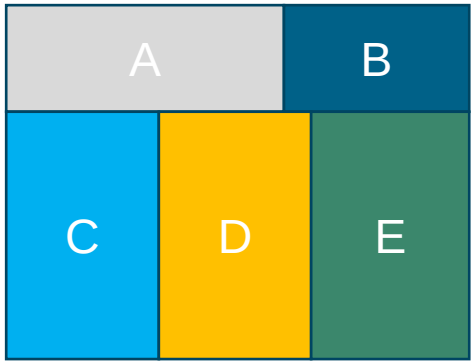
Si-Interposer



Reconstituted Fan-Out

Drivers for Chiplet Integration

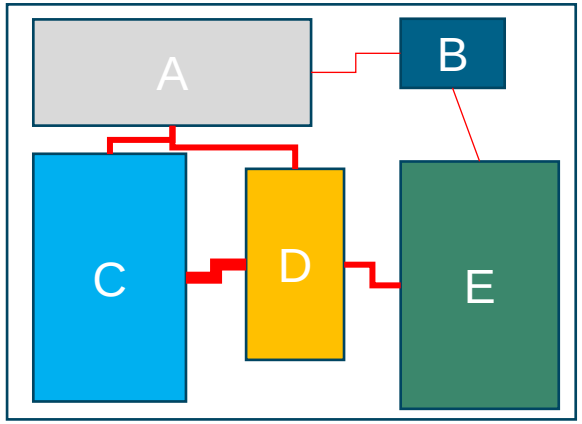
SOC



- Difficult
- Very Costly
- Low Initial Die Yield

End of Cost Advantage of Moore's Law

Shared Package



Pros

- **SWAP**
- Flexibility
- Optimized Performance
- Lower Power
- Shorten Time-to-Market
- Gordon Moore predicted that eventually one would go to packaging individual chips – Original paper.
- Thermal optimization
- Spin multiple products faster

Cons

- **Create System Integration Ecosystem (Supply Chain and Business).**
- KGD – Known Good Die
- Establish a pull by customers
- Standards
- Software Design Tools
- Yield Loss Ownership

Moore's Law is Dead – Long-live the Chiplet!

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SkyWater Technology

- The first U.S.-based pure-play service provider of silicon interposer, FOWLP, and hybrid bonding HI technologies
- Unique silicon process capabilities being established to support 2.5D/3D microsystems for commercial and government customers
- ITAR registered with workspaces and fab facility capable of supporting secure applications (Cat. 1A Trusted Accreditation in progress)
- Strategically leverages a not-for-profit, industry-friendly public-private partnership with BRIDG (Bridging the Innovation Development Gap) to accelerate technology commercialization and the USG, as well as linking with higher education for workforce development and research

OPERATION

200 mm equipment
Size: 109,000 ft^2 total
26,000 ft^2 of class 1000
9,400 ft^2 of class 10,000

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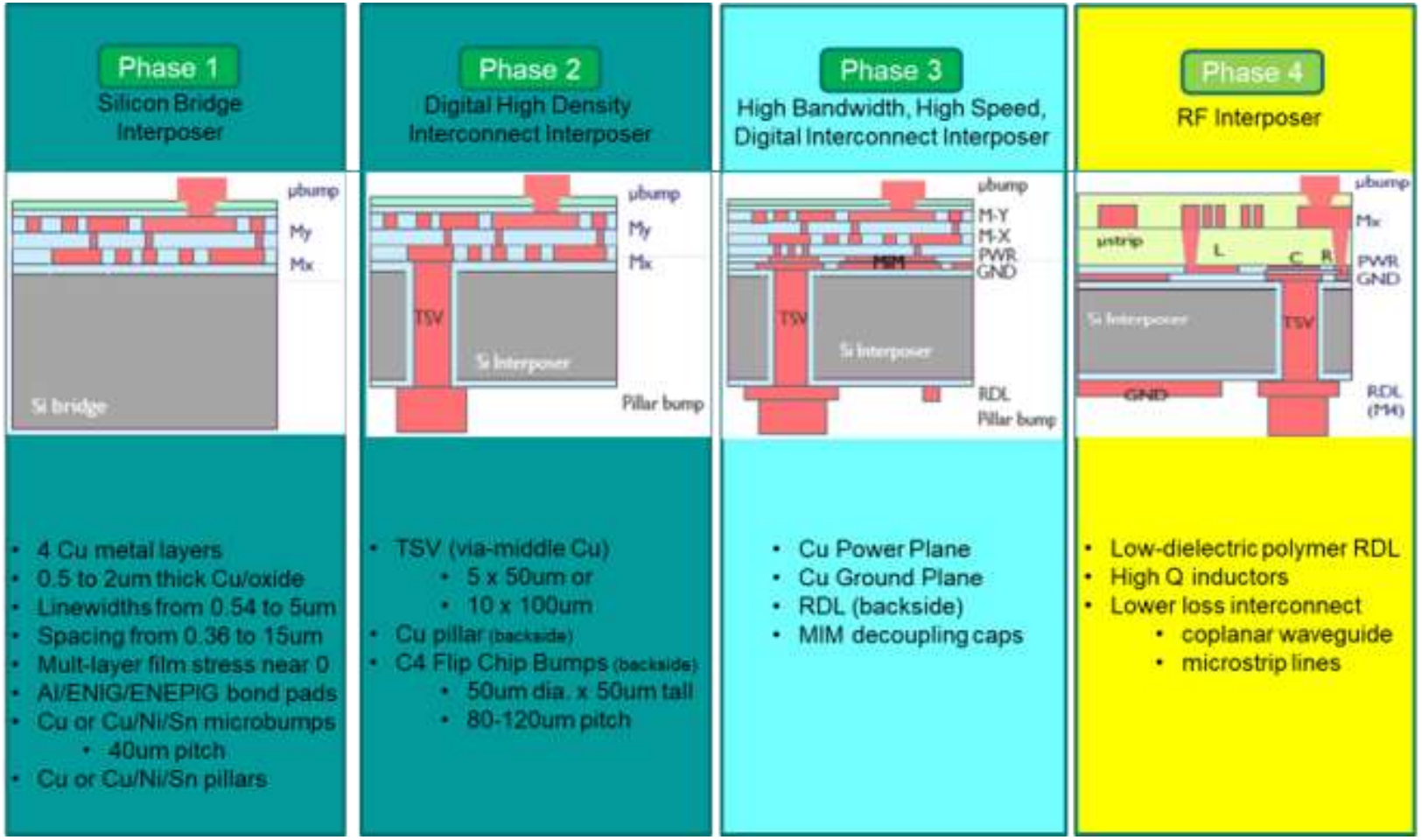
Silicon Interposer Development

- Based on technology license from IMEC and funded by an IBAS program awarded to BRIDG
- Phase 1 completed and Phase 2 underway with target to complete 1H2023
- Multiple follow-on demonstrator programs are in place
- Later phases focus on extending the initial process to include more routing layers and an RF version



Capacity and capability expansion in the future to support higher volume

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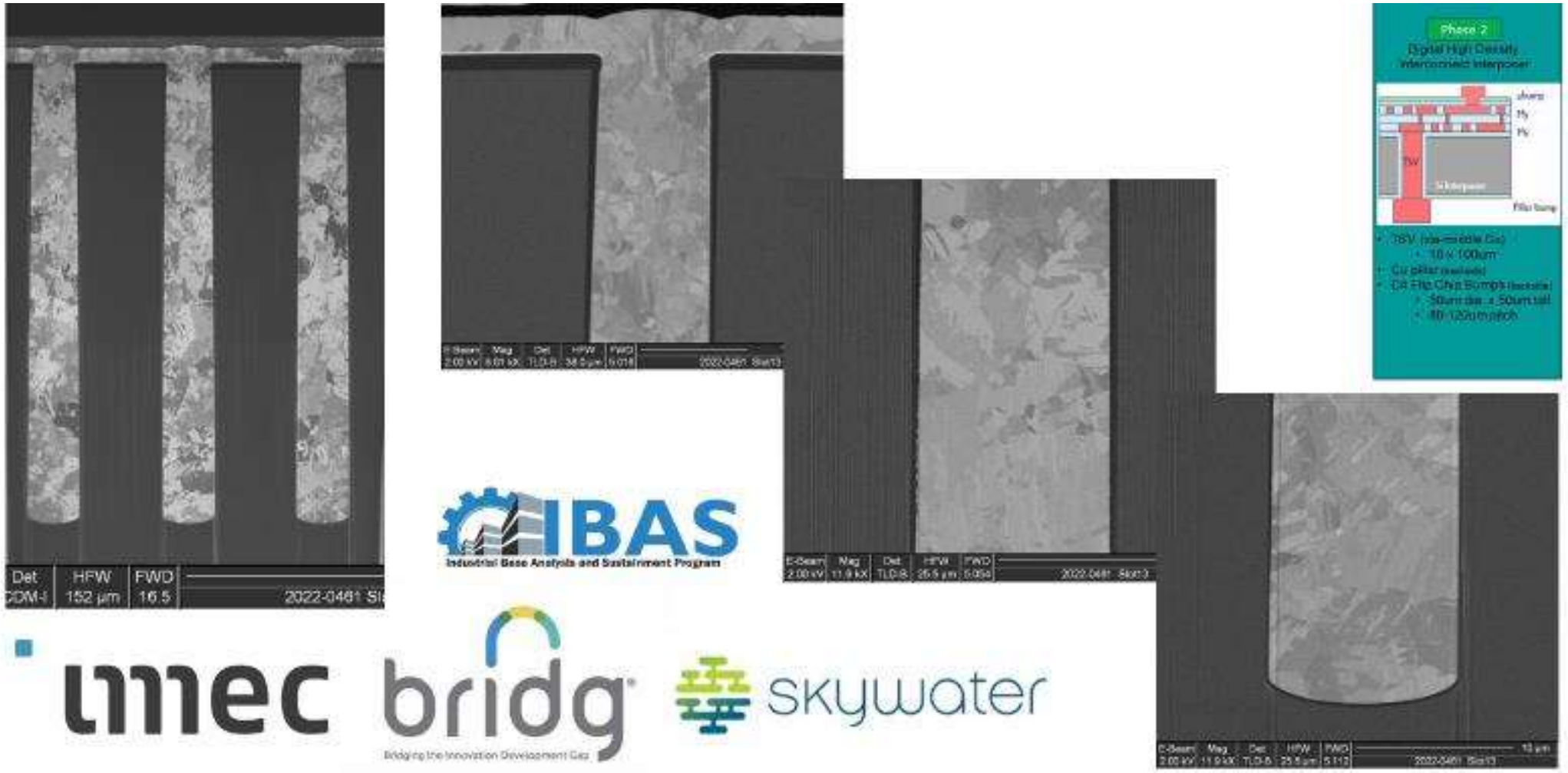
Silicon Interposer – TSV



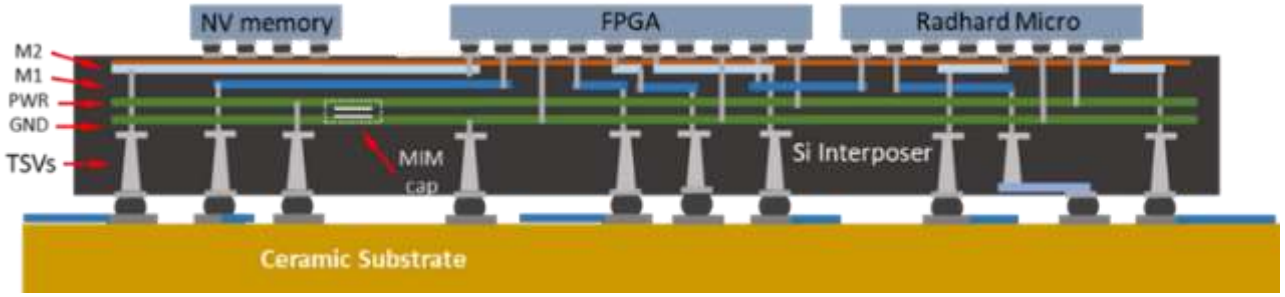
Silicon Interposer Technology & Roadmap

Technology Details

- Max reticle size: 22mm x 22mm
- TSV size: 10um x 100um (10:1 AR)
- TSV metal: Electroplated Cu
- Topside metallization: up to 4 layers, damascene
- Backside: RDL & Solder Bumps
- Daisy chain and functional hardware designs
- Design rule manual (currently in beta version)

Roadmap

- Phase I – Qualified Q2/2022
- Phase 2 & 3 – Q1 2023
- Phase 4 – Target qualification date Q3 2023
- Potential future ability to support TSV-last insertion into finished CMOS devices that have been designed with keep-out areas for TSVs



Schematic Courtesy of BRIDG

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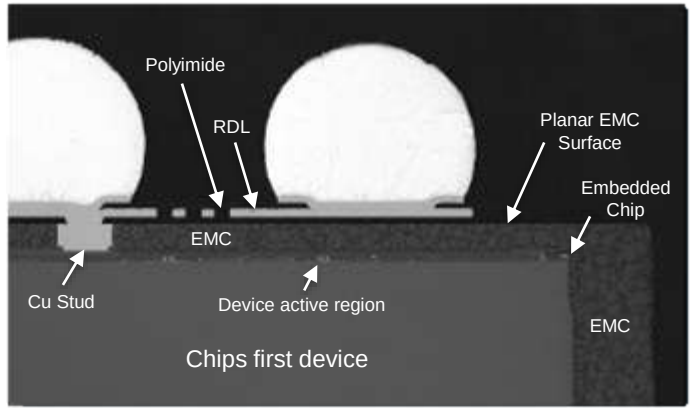
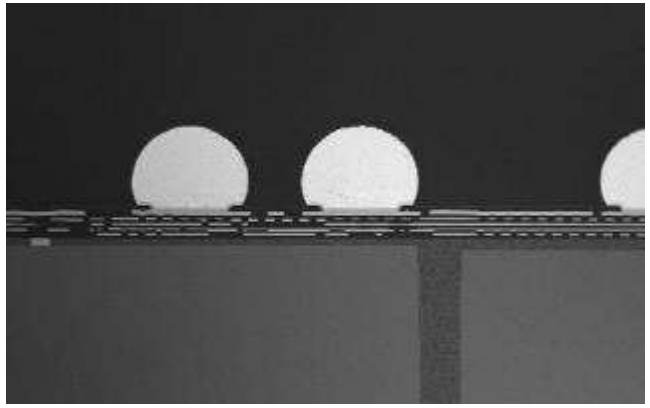
Deca M-Series™ FOWLP Technology Development

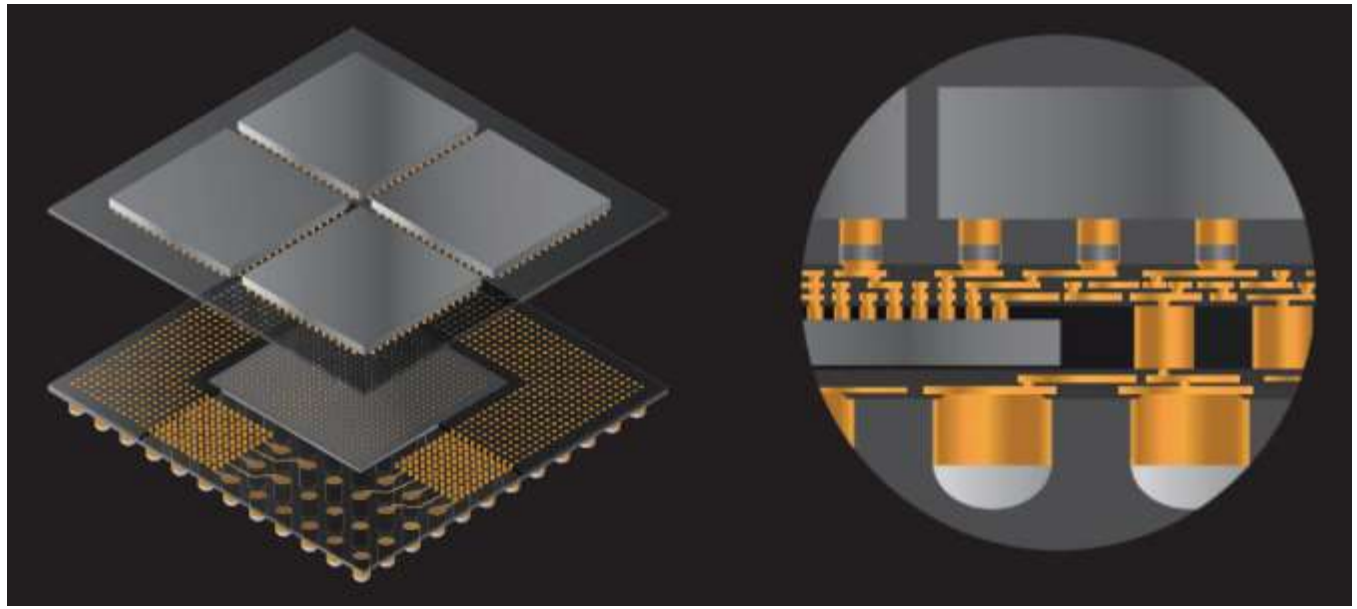
- Chips-first, chips-up fan-out technology with fully encapsulated active region
- Provides flexible heterogeneous integration platform with embedded chips-first and chips-last options
- Enables IO footprint extension beyond Si device area with ability to integrate disparate devices in a single package
- SkyWater is the 3rd Deca licensee and only U.S.-based company
- Why Deca M-Series?
  - Highest volume FOWLP technology in production today
  - Superior reliability and yield
  - Adaptive Patterning enables ultra-high-density scaling to 20µm IO die pad pitch & 2µm line & space with Gen 2

Single Die – Single RDL



Multi Die – Multi layer RDL





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Deca M-Series FOWLP Technology Roadmap

M-Series Gen 1

2016 →

Codec

RF

IoT Device

PMIC

Dual PMIC

Single-die

- Protected fan-in
- Fan-out

Multi-die

- RF & IoT modules
- Integrated PMICs

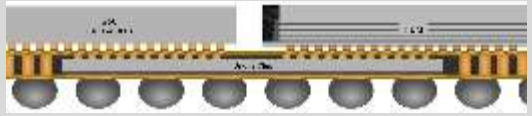
55 µm bond pad pitch
8 µm lines & spaces
Up to 2 layers of RDL

M-Series Gen 1.5

(High Density Integration)
2021 →

1. 3D PoP - Mobile Applications Processor

2. Fan-out Chip on Substrate – Bond pad pitch expansion on advanced node Si



3. Embedded Bridge Die Interposer – Replacing Si interposers for SoC to HBM integration

4. Passive & Active Interposers – Power mgmt., memory integration, etc. for CPU, GPU, AI & Networking

45 µm bond pad pitch
5 µm lines & spaces
Up to 5 layers of RDL

Gen 2 (SkyWater FL)

(Ultra-High-Density Integration)
2023 →

- 20µm die pad pitch
- 2µm lines & space
- 2.5D embedded die interposers
- 3D structures
- Embedded bridge die
- RDL-only ultra-high-density interposers

Ultra-high-density chiplet integration

No reticle = No package size limitation

20 µm bond pad pitch
2 µm lines & spaces
> 5 layers of RDL

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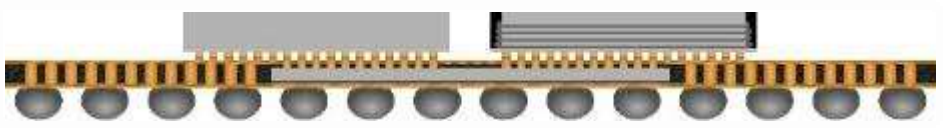
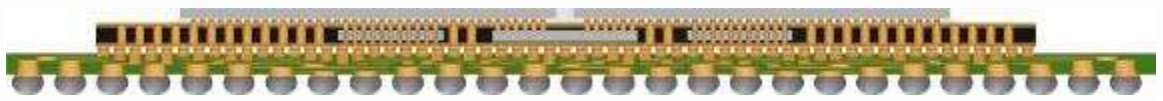
Deca M-Series FOWLP Summary

- 200mm demo test vehicle completion on plan for early Q1 2023
- Gen 2 technology implementation in 2023
- Initial customer processing engagements in late 2022 – early 2023



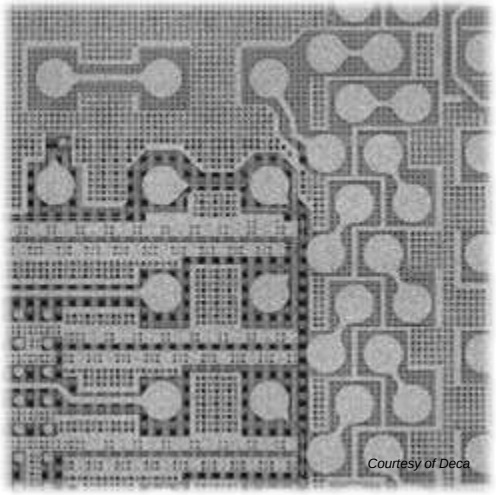
Molded Bridge Die Interposer



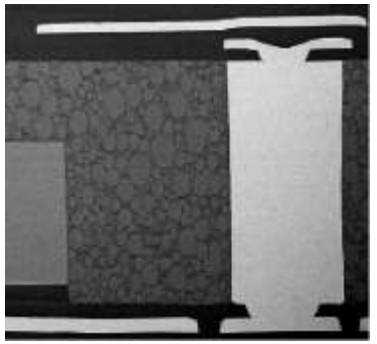
Bridge & IPD – chips last SoCs

Bridge & IPD – chips first SoCs

No Bridge Die – chips first or chips last



Actual M-Series multi-layer device
(Post-RDL, pre-UBM)



Actual 3D M-Series
(Thru-mold Cu posts with dual-sided RDL)

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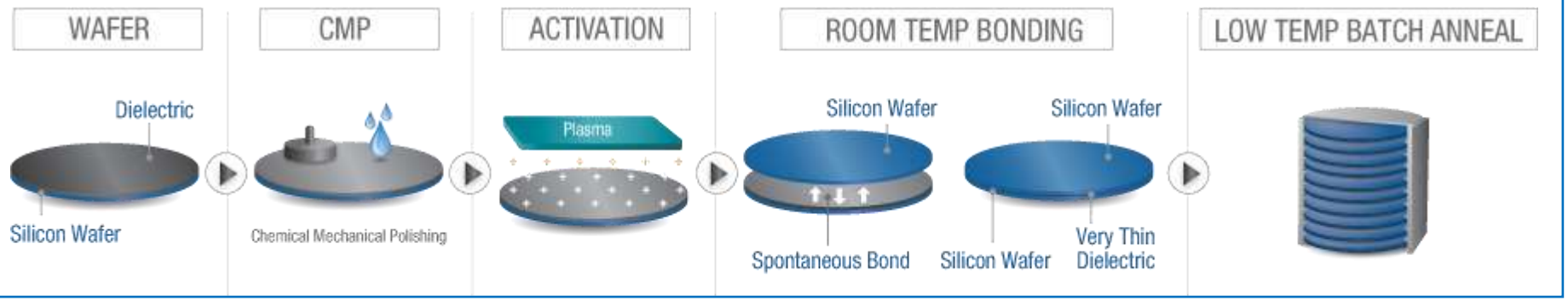
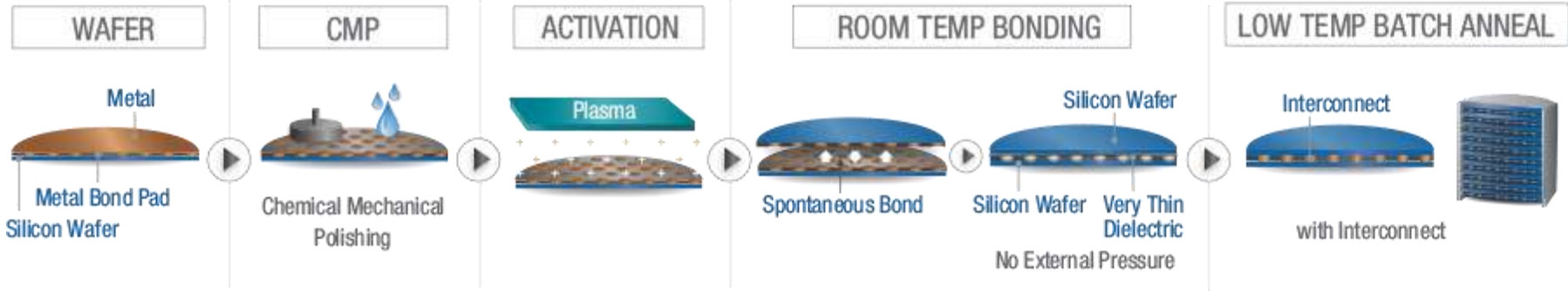
Hybrid Wafer Bonding

Adeia ZiBond® technology: hybrid bonding **without** electrical interconnect





Adeia DBI® technology: hybrid bonding **with** electrical interconnect

SkyWater licensed the Adeia ZiBond® and DBI® wafer-to-wafer bonding technologies in May 2022

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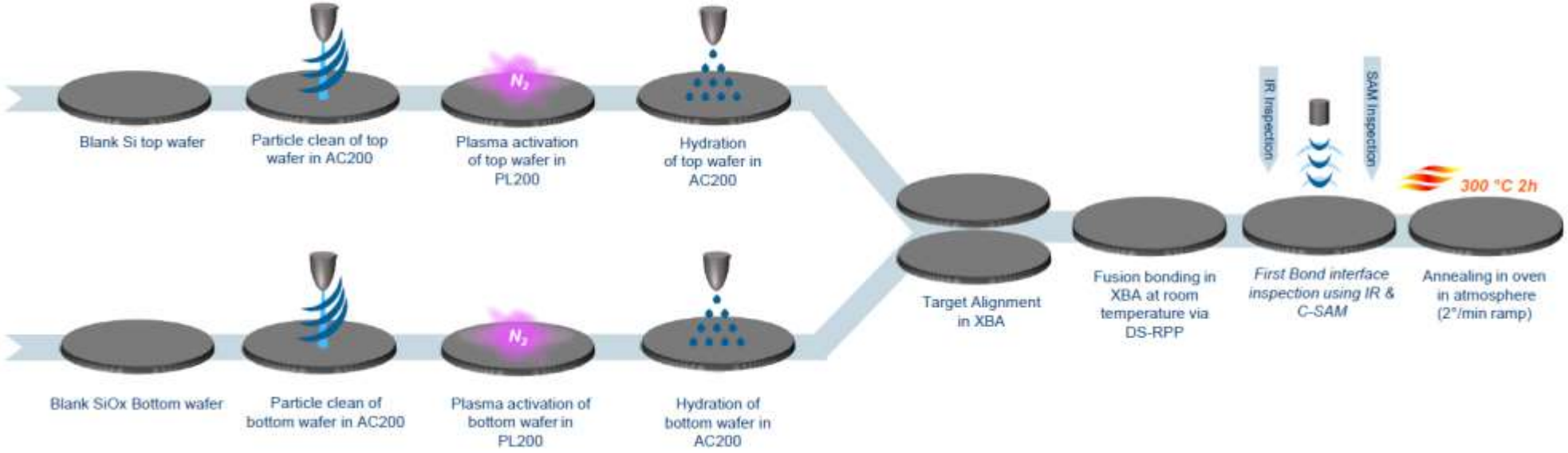
Hybrid Wafer Bonding

XBS200 Bonding Platform

- Single 6-axis robot with tool exchanger
- World‘s first fixture-less automated bond platform
- Offers unique features such as laser pre-bond
- Covers all MEMS bonding processes
- System incorporates laser pre-bond, high precision bond aligner, aqueous cleaner, plasma activation module, and overlay meas.



Hybrid Wafer Bonding

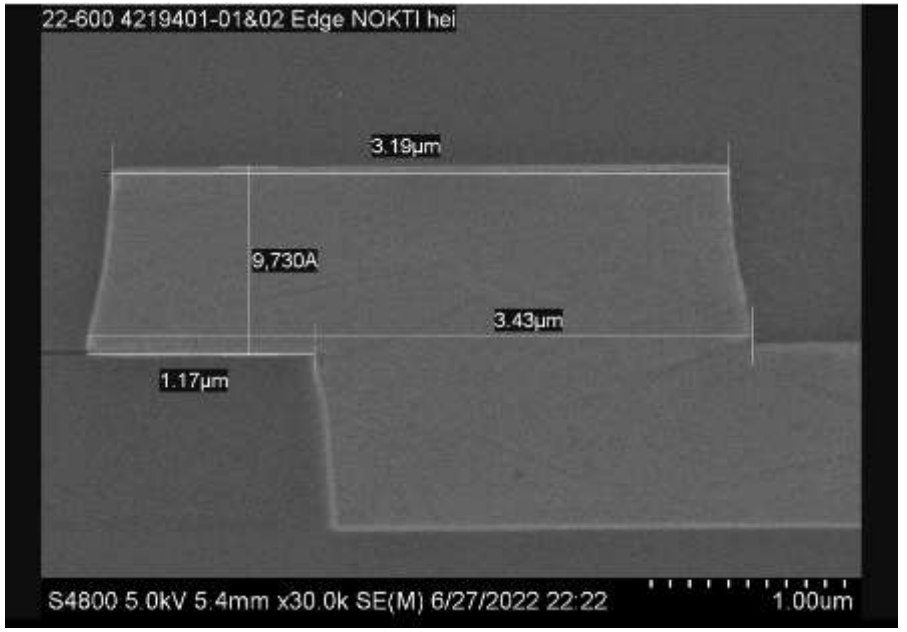
Technology Capability

- 200mm wafer bonding platform capability
- Bonding performed at room temperature to eliminate CTE-driven misalignment
- Support for high density interconnect at small pitch
- Enables extremely short interconnect length

Roadmap

- Zibond® & DBI® tech transfer – Q1 2023
- Future interests in
  - 300mm wafer bonding (new infrastructure for interconnect processing and bonding)
  - Die-to-wafer hybrid bonding

Initial Hybrid Bonding Demo from XBS200



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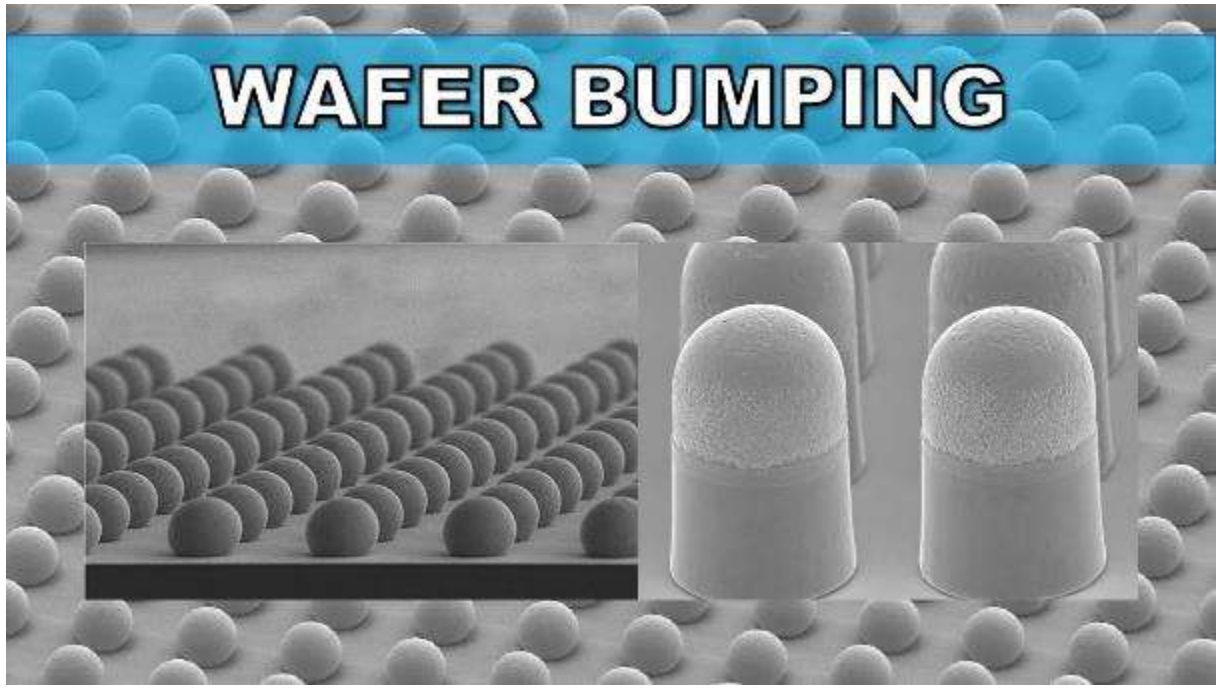
Wafer Bumping

Image Courtesy: Semicon Talk



- Wafer bumping is a ubiquitous need in advanced packaging
  - Nearly all advanced package architectures incorporate bumps at some level
- Lack of 300mm capability in the US
  - Essentially no non-captive 300mm capability and sources of 200mm capability are becoming fewer
  - On the opposite end of the spectrum, support for smaller wafer sizes and non-silicon substrate materials is also limited
- Bumping technologies encompass a wide variety of materials, structures, and dimensions
  - WLCSP bumping for package/module-to-board attach
  - C4 for flip chip applications (laminates, interposers)
  - Cu pillar for high density, fine pitch interconnect (advanced laminates, interposers)
  - Need to support Pb-based and Pb-free solder alloys
  - May also include RDL processes if redistribution is needed to convert device I/O layout to a new footprint

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Backend Processes, Assembly, and Test

- Backend processes include wafer thinning, dicing (mechanical, plasma, laser), temporary bond/debond, sort, and final inspect
  - Several U.S. companies offer these services, but capacity expansion will be needed to support a growing domestic market
  - Companies engaged in AP&HI need broad capabilities to handle varying substrate materials, thin die or die with fragile exposed structures,
- Assembly
  - Advanced assembly capabilities that can support 2.5/3D architectures (multi chip/chiplet modules, interposer-based devices, stacked device structures) need to be established for higher volumes and varying device technologies
- Testing
  - Wafer level test after fab or bumping to identify KGD prior to backend processes
  - Module level testing, particularly in the middle of assembly flows, is challenging
  - Reliability testing with a wide array of thermal, mechanical, and environmental options

Ideally, all these capabilities would exist in a single provider/location for sensitive or secure applications

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Keys to Establishing a Domestic Manufacturing Ecosystem

- Develop broad consensus and priorities on the packaging technologies and capabilities that need to be established
- Align U.S. gov't business engagement process and funding practices with commercial industry expectations and needs
- Consolidate and forecast U.S. gov't full lifecycle demand and technology needs to align with the industry's forward-looking financial planning
- Expand existing and develop new, pre-competitive Public-Private Partnership organizations in workforce development, R&D, design, fabrication, packaging, and test infrastructure involving both academia and industry
- Fully leverage existing onshore assets and expand and improve on current infrastructure and workforce to optimize outcome
- Develop Baseline metrics to support accurate assessments of program-wide progress towards economic and security objectives and to highlight remaining gaps that may require other support

Acknowledge that the CHIPS act is a good start, but continued investment will be needed to establish a comprehensive manufacturing ecosystem

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Thank You!

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